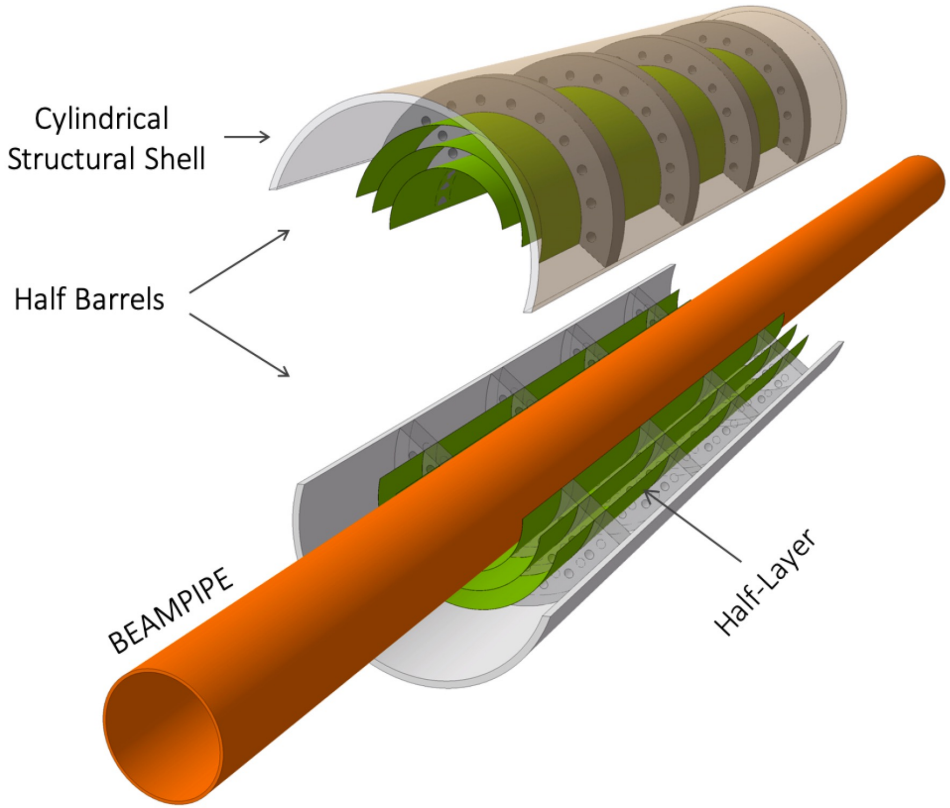


ITS3 for ALICE

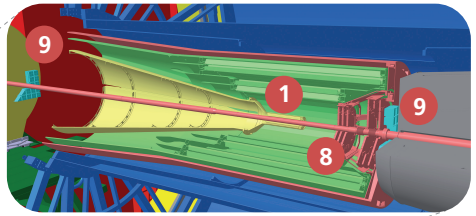
Sanghoon Lim
(Pusan National University)
on behalf of the ALICE collaboration

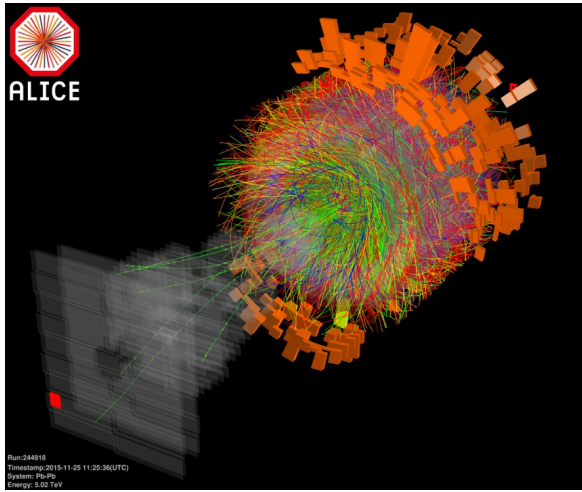
APCTP Workshop
on the Physics of Electron-Ion Collider

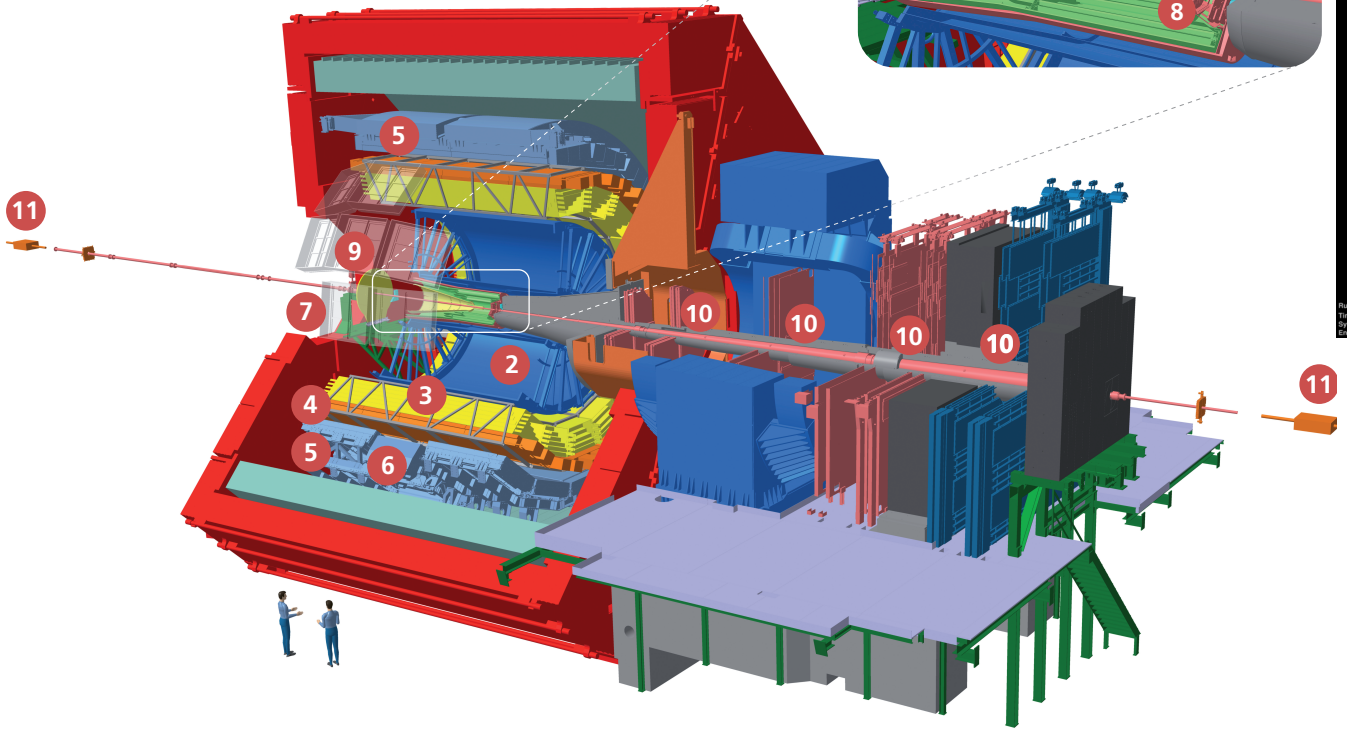
ALICE

PUSAN NATIONAL UNIVERSITY

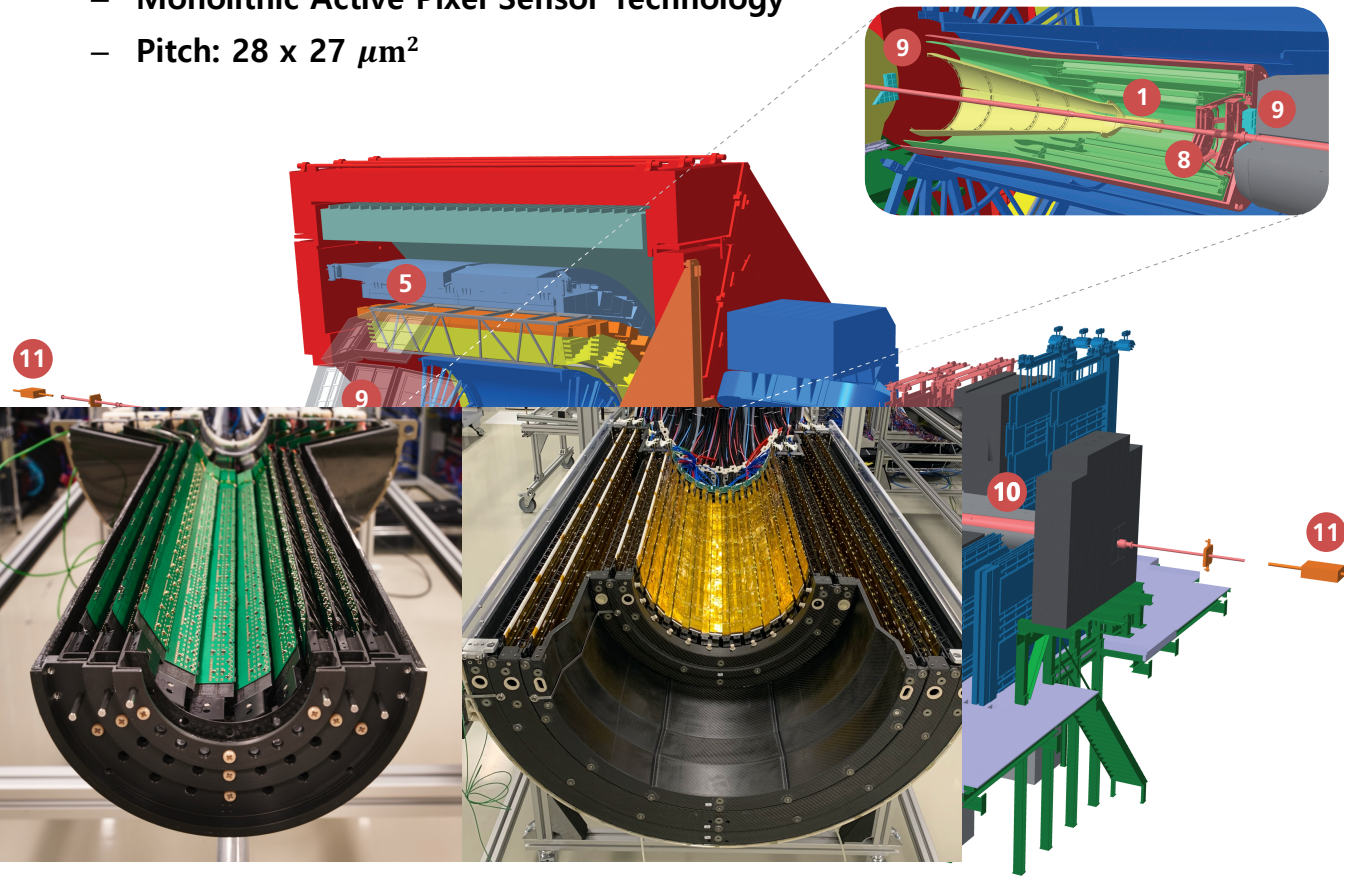
- **Study of properties of quark-gluon plasma in heavy-ion collisions**
  - **Charged particles at low p_T**
  - **Charm and bottom hadrons**

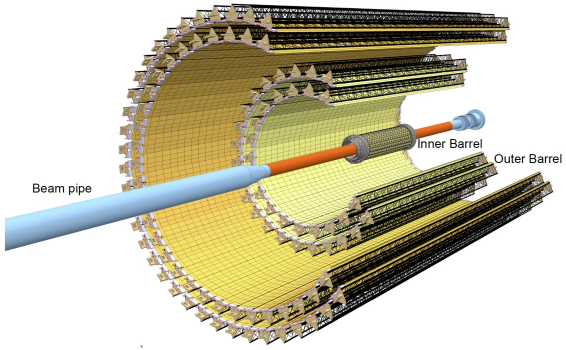






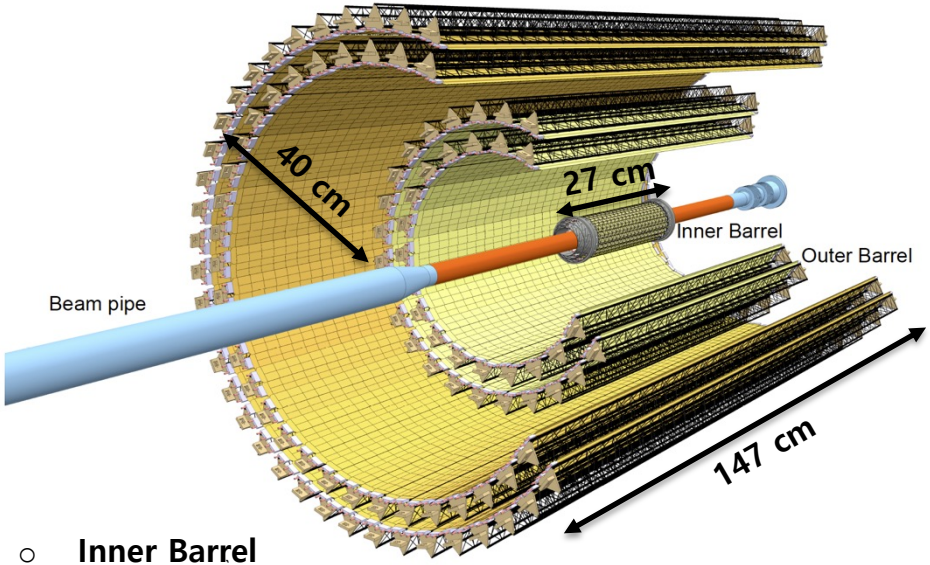
- New inner tracking system (ITS2) for Run 3
  - Monolithic Active Pixel Sensor Technology
  - Pitch: 28 x 27 μm^2

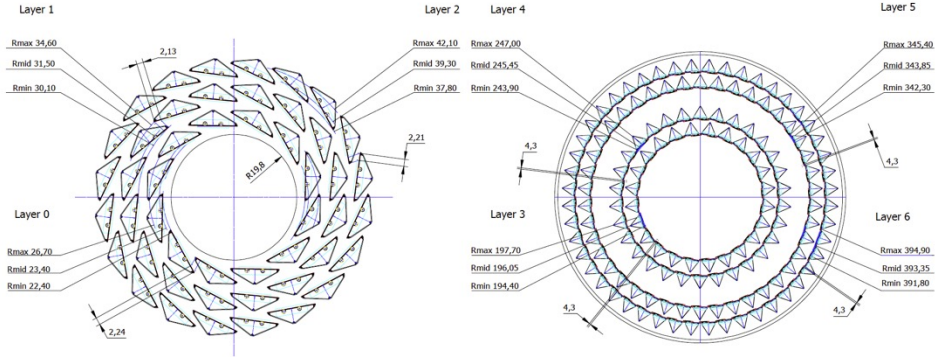


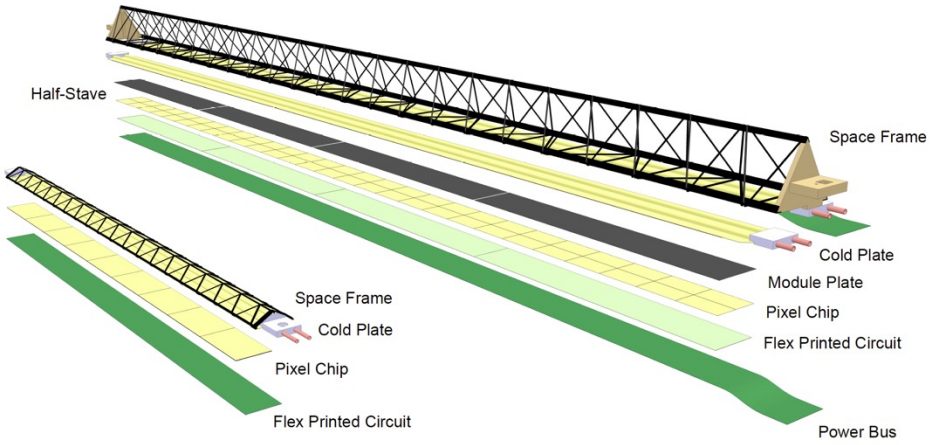


- 7 layers
- All silicon pixels
- Chip thickness
  Inner 3 layers: 50 μm
  Outer 4 layers: 100 μm
- Rate capability
  100 kHz Pb+Pb

- **New inner tracking system (ITS2) for Run 3**
  - **Monolithic Active Pixel Sensor Technology**

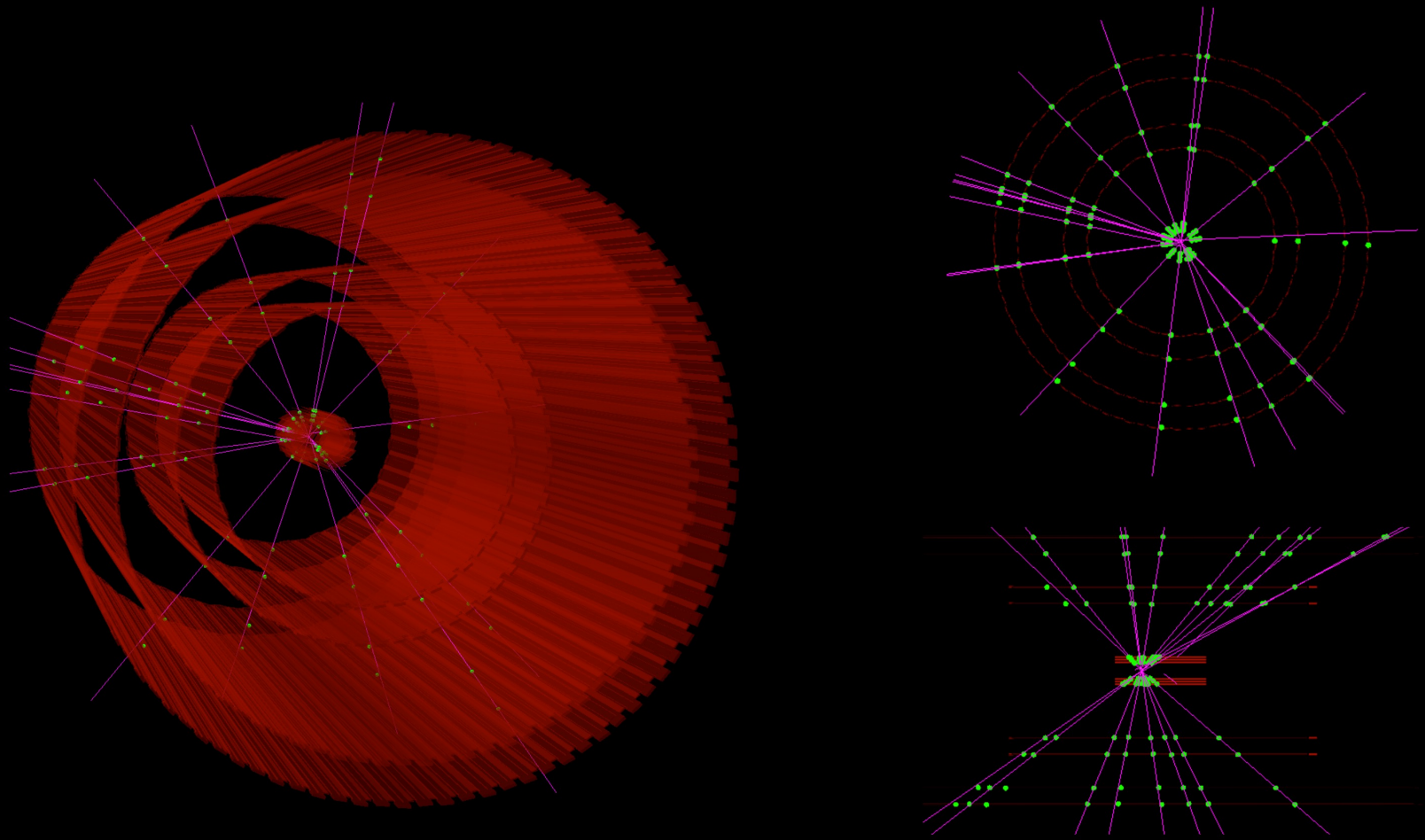




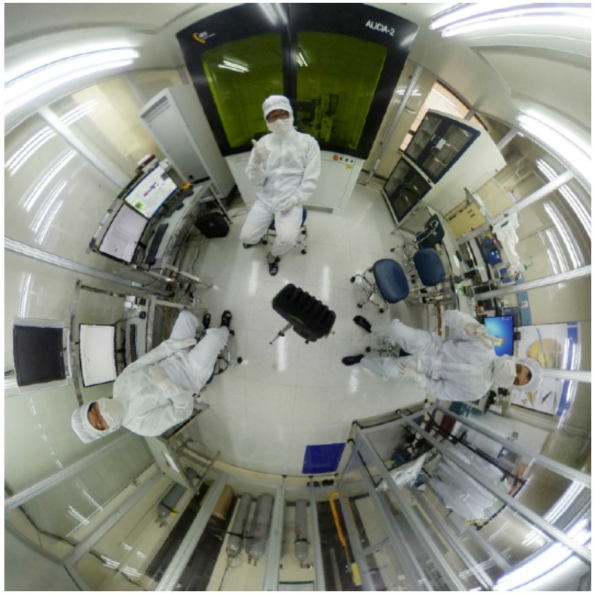


- **Inner Barrel**
  3 layers: 12+16+20 staves
  9 sensors per stave
- **Outer Barrel**
  2 middle layers: 30+24 staves (2x4 modules/stave)
  2 outer layers: 42+48 staves (2x7 modules/stave)
  2x7 sensors/module

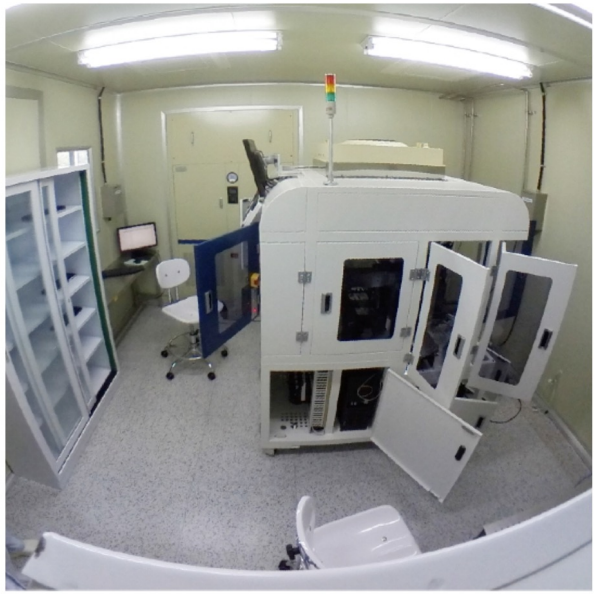
LHC pilot beam (900 GeV proton collisions)



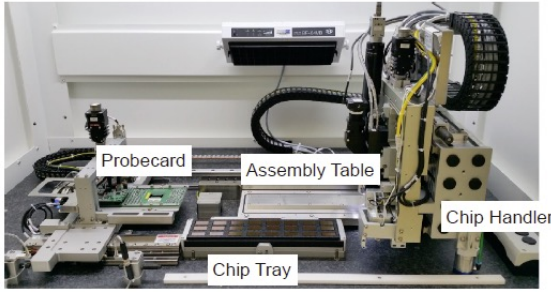
KoALICE contribution to the ALICE ITS2



PNU/Inha University



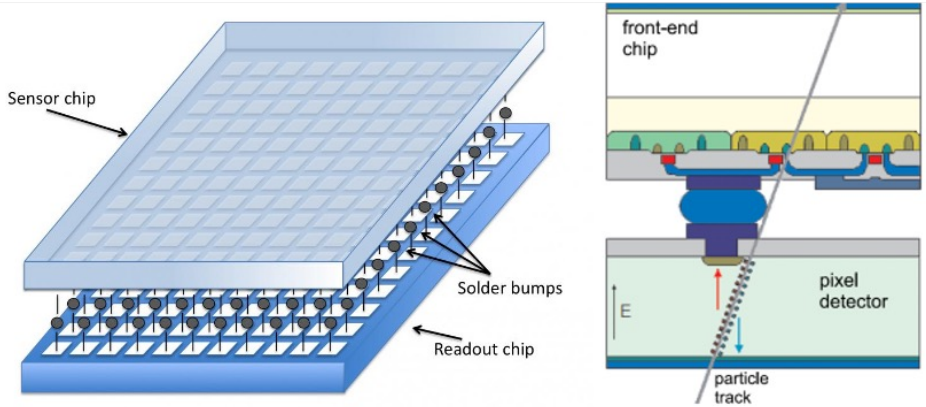
Yonsei University



- Design of Pixel Sensor Chip
- Characterization of Pixel Sensor Chip
- Chip production (thinning & dicing)
- Chip test
- Detector module production and test

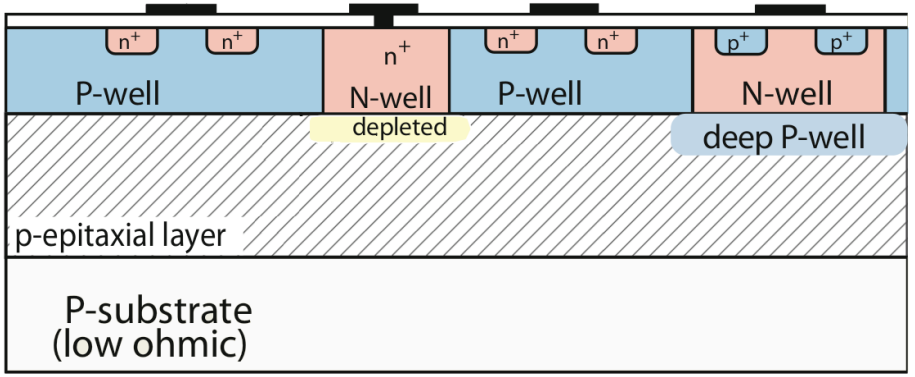
Monolithic Active Pixel Sensor (MAPS)

Hybrid
: Sensor and readout electronics separated



- Majority of currently used silicon detectors
- Possible to optimize sensor and readout electronics separately
- Large power consumption and material budget

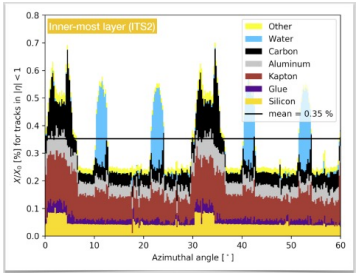
Monolithic
: Sensor and readout electronics integrated



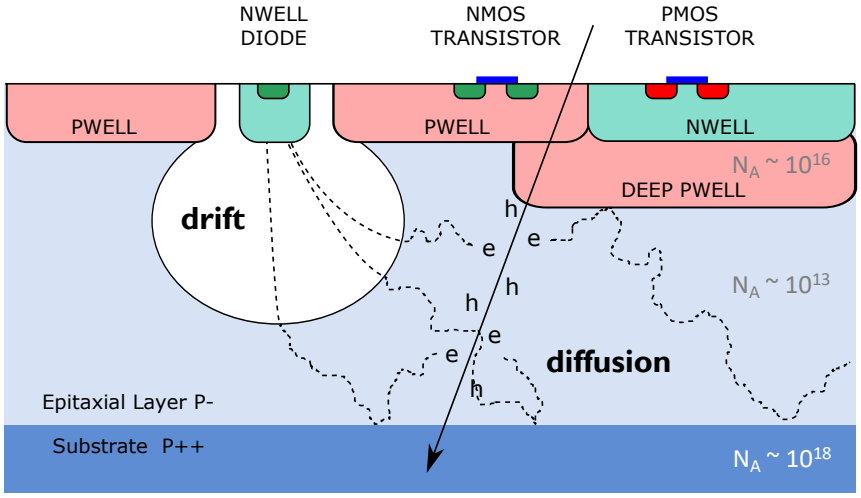
- Recently developed and used (first generation for STAR HFT)
- Easier integration
- Lower power consumption and material budget

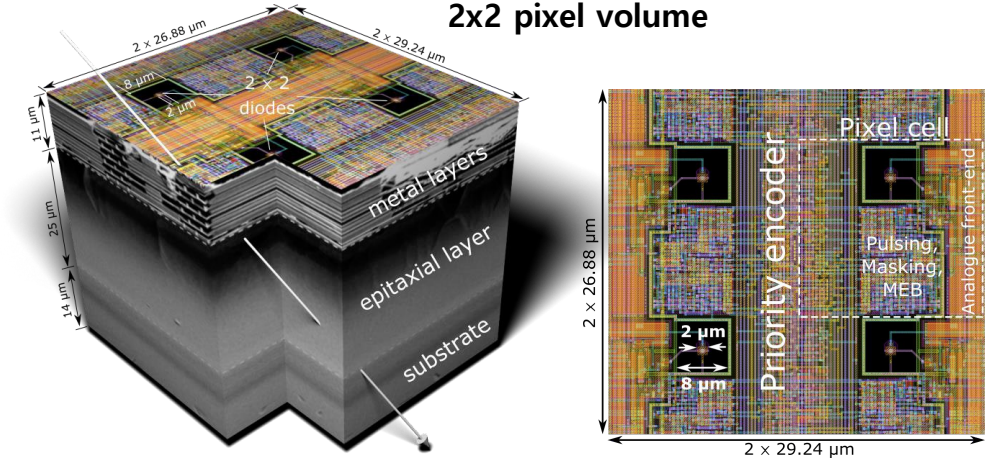
  1.14% X_0 per layer

  → 0.35% X_0 per layer

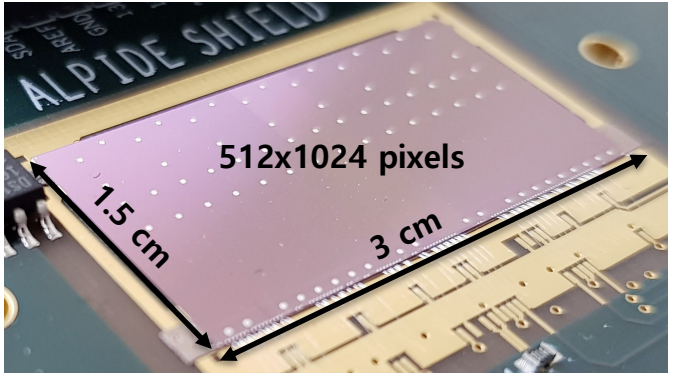


- **CMOS pixel sensor using 180 nm CMOS Imaging Process**

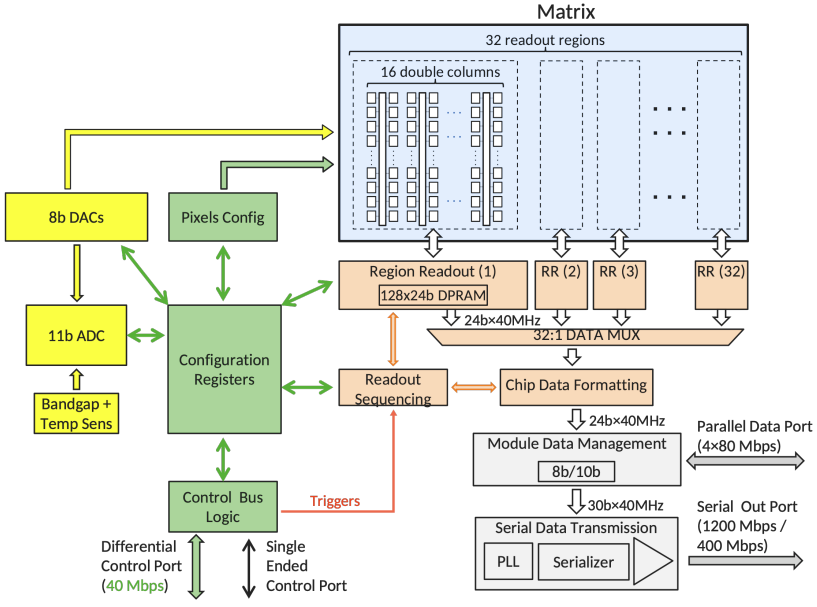


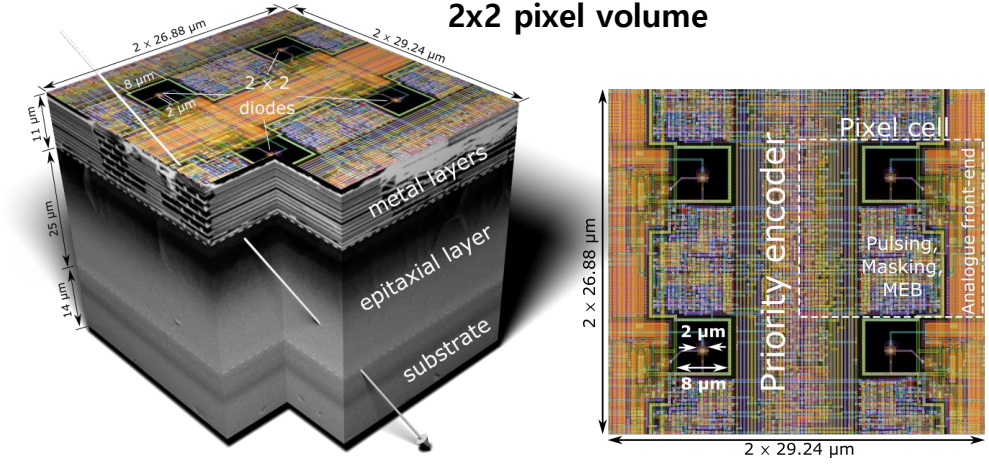


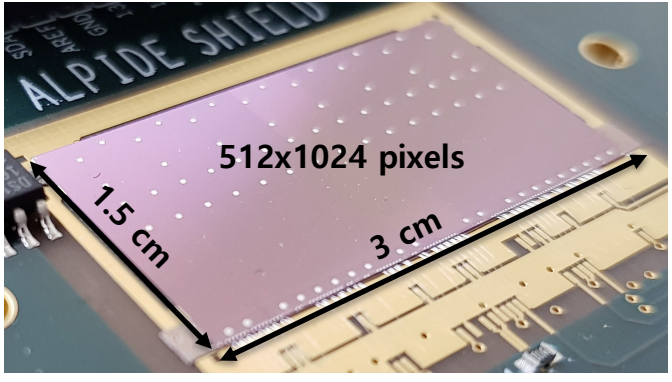
- High-resistivity (>1 $k\Omega$ cm) p-type epitaxial layer (25 µm) on p-type substrate
- Small n-well diode (2 µm diameter) ➔ low capacitance (~5 fF)
- Reverse bias voltage (-6 V<V_{BB}<0 V) to substrate to increase the depletion region (<30 ns charge collection time with V_{BB} =-3 V)
- Deep p-well shields n-well of PMOS



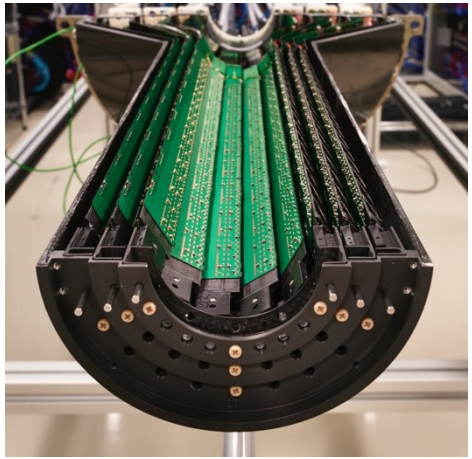
- **Fully integrated signal processing**

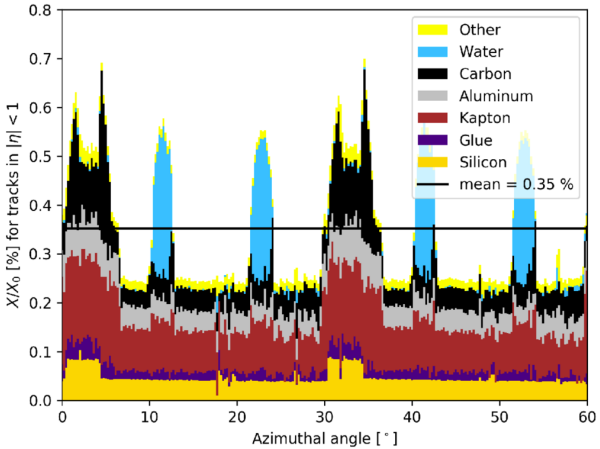


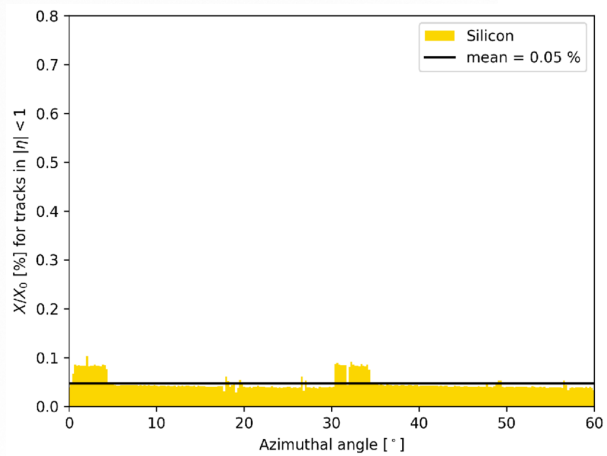


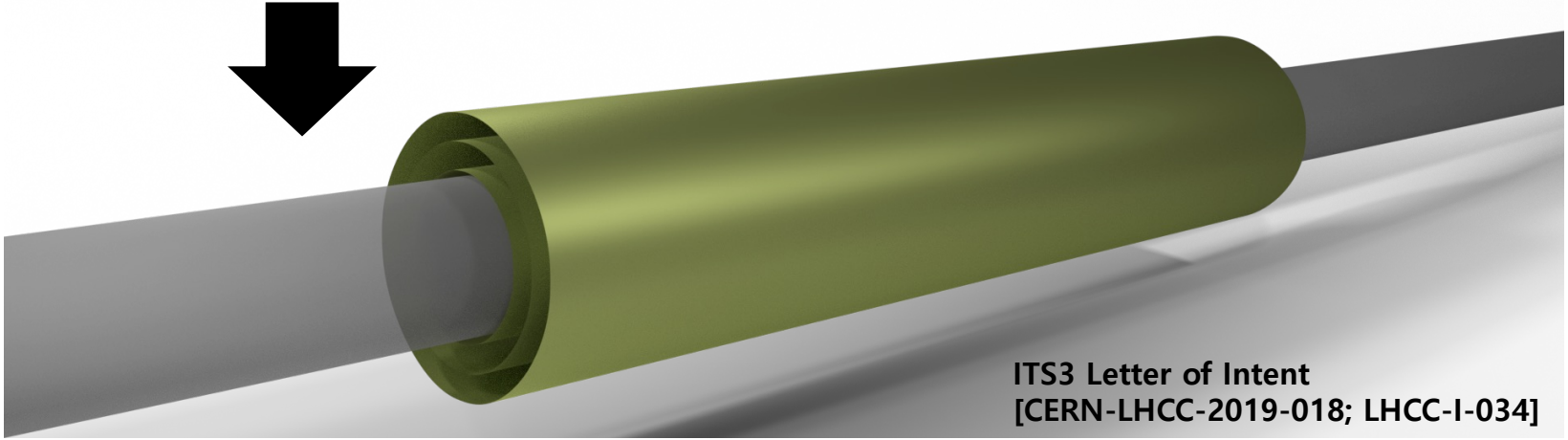


- **Front-end**
  shaping time: <10 µs
  power consumption: ~300 nW/pixel (<40 mW/cm2)
- **Multi-event memory: 3 stages**
- **Fake-hit rate: <1 Hz/cm2**
- **Triggered or continuous readout mode**

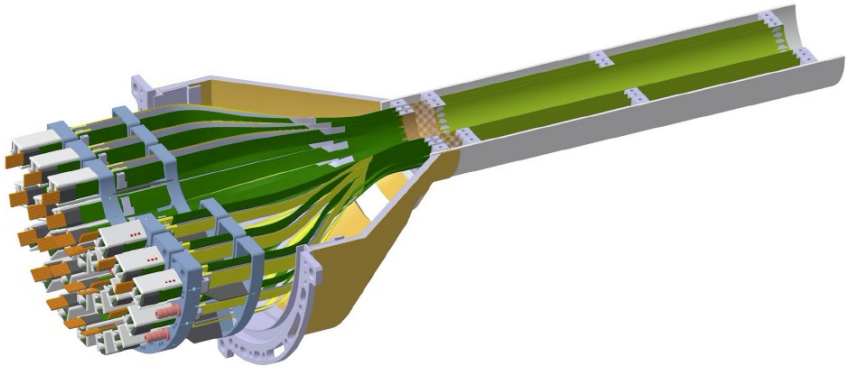



Other
Water
Carbon
Aluminum
Kapton
Glue
Silicon
mean = 0.35 %
X/X0 [%] for tracks in |η| < 1
Azimuthal angle [°]


Silicon
mean = 0.05 %
X/X0 [%] for tracks in |η| < 1
Azimuthal angle [°]

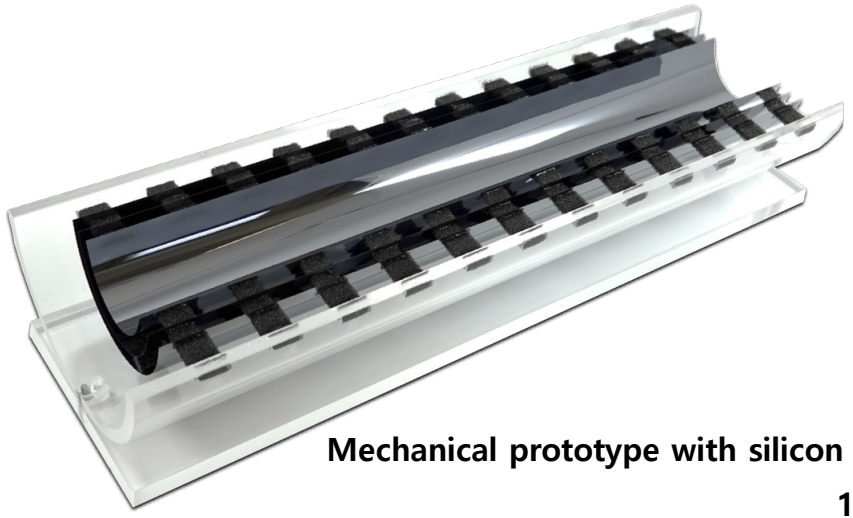

ITS3 Letter of Intent
[CERN-LHCC-2019-018; LHCC-I-034]

- **Closer to the interaction point and less material**



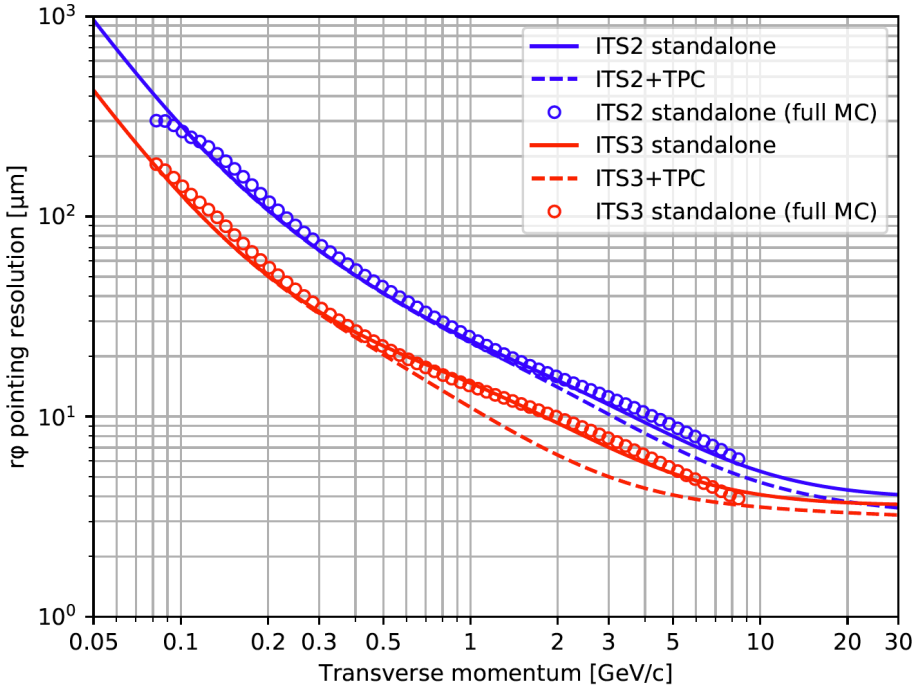
- 300 mm wafer-scale sensors using stitching technology
- Very thin (20-40 μm) sensors
  ➔Low material budget (0.02-0.04% X_0 per layer)
  ➔Flexible enough to be bent
- Carbon foam ribs for mechanical support

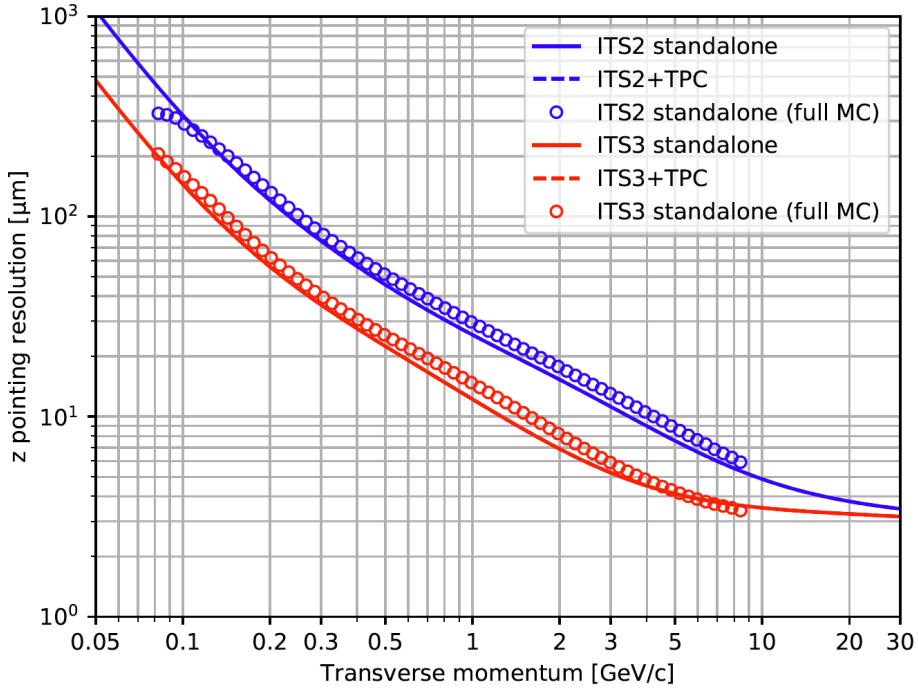
Beam pipe Inner/Outer Radius (mm)	16.0/16.5		
IB Layer Parameters	Layer 0	Layer 1	Layer 2
Radial position (mm)	18.0	24.0	30.0
Length (sensitive area) (mm)	300		
Pseudo-rapidity coverage	±2.5	±2.3	±2.0
Active area (cm^2)	610	816	1016
Pixel sensor dimensions (mm^2)	280 x 56.5	280 x 75.5	280 x 94
Number of sensors per layer	2		
Pixel size (μm^2)	O (10 x 10)		



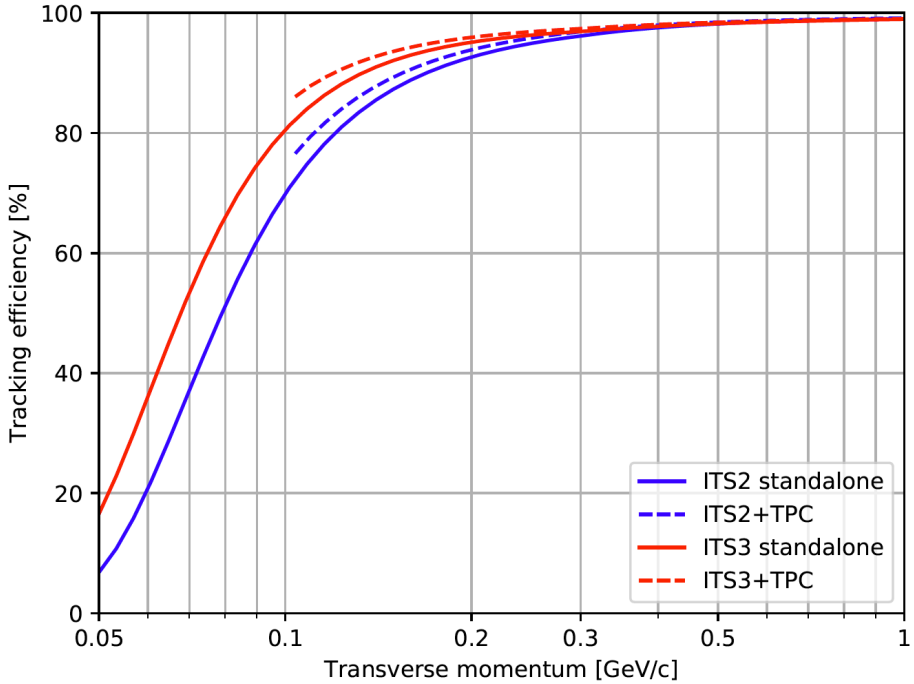
Mechanical prototype with silicon

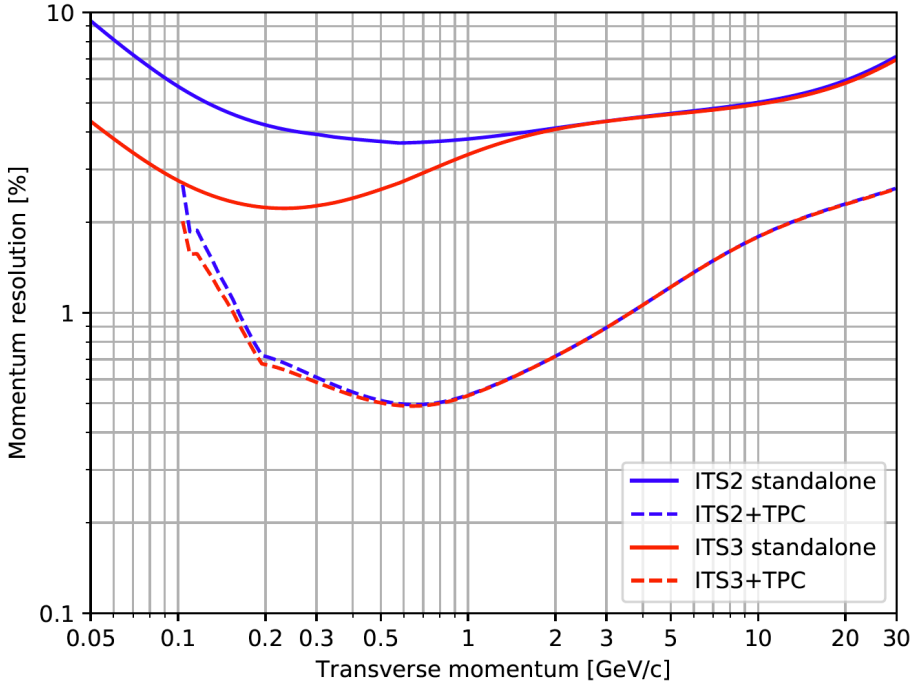
- **Pointing resolution**

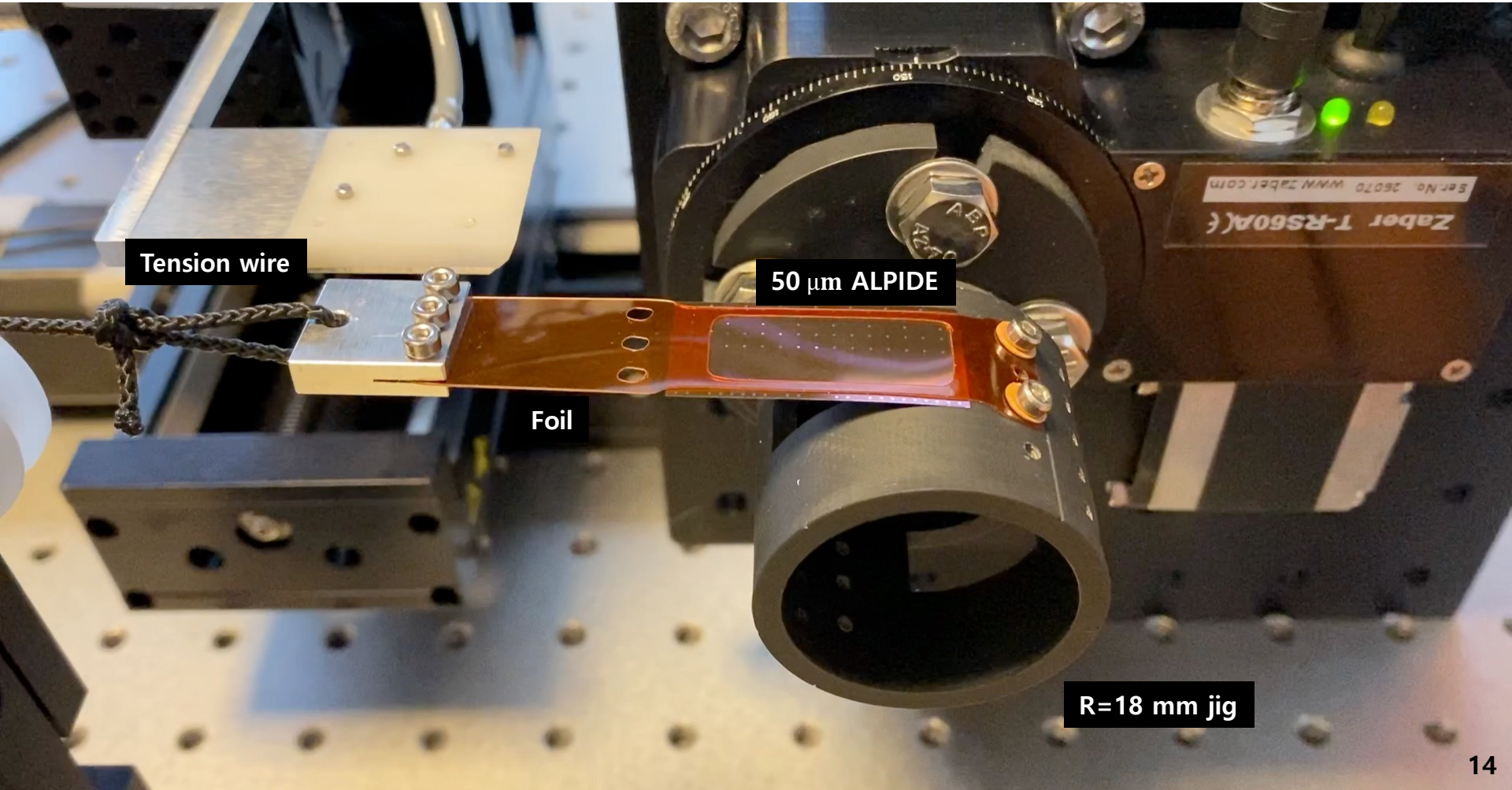




- **Tracking efficiency and momentum resolution**






Tension wire
50 μm ALPIDE
Foil
R=18 mm jig

Test beam with bent chip

- **First test beam with bent chips in Aug 2020 (DESY)**
  - **Proved that bent chips are working with excellent efficiency**

arXiv:2105.13000

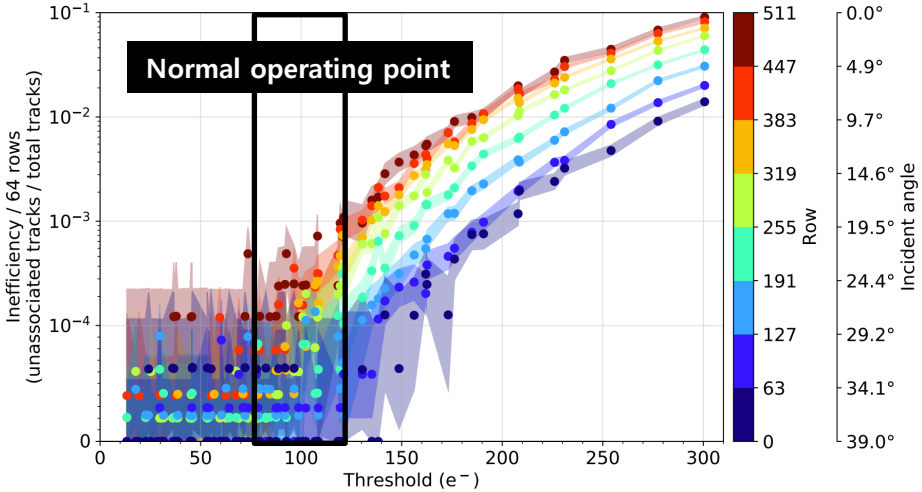
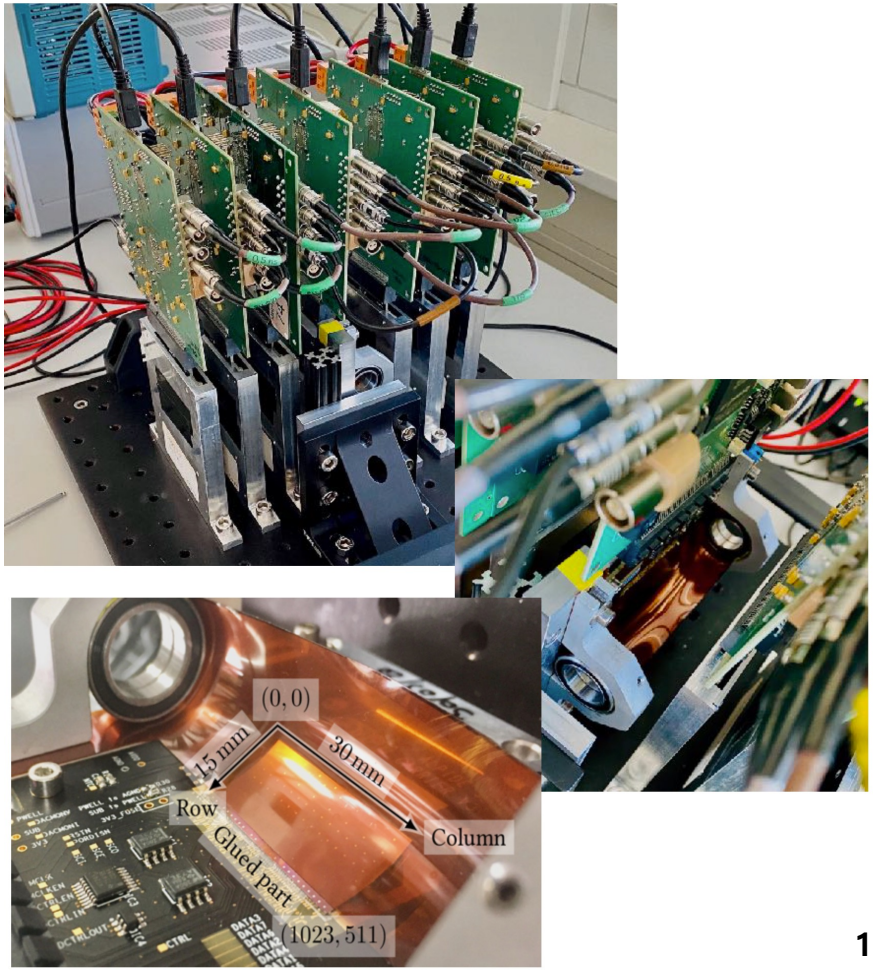
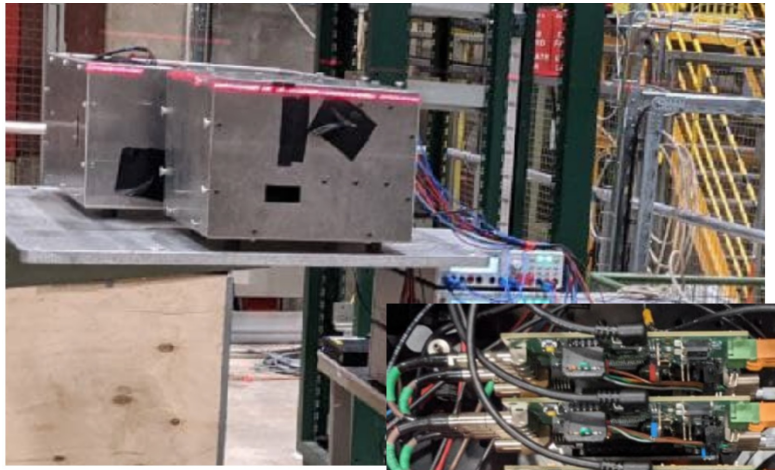


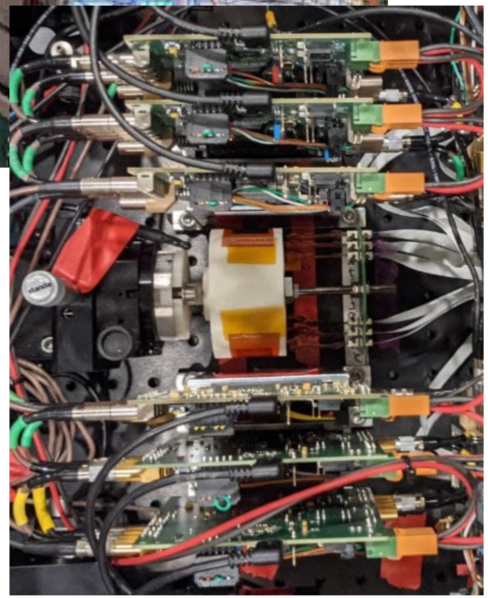
Figure 10: Inefficiency as a function of threshold for different rows and incident angles with partially logarithmic scale (10^{-1} to 10^{-5}) to show fully efficient rows. The dark circles represent the calculated efficiency and the shaded areas the statistical uncertainty. Each data point corresponds to at least 8k tracks.

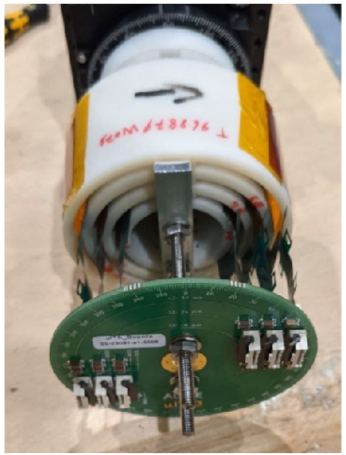


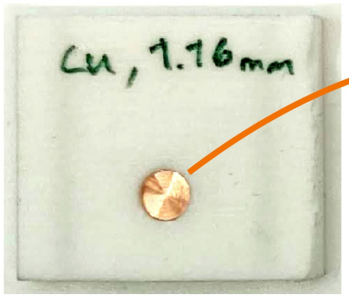
Test beam with bent chip

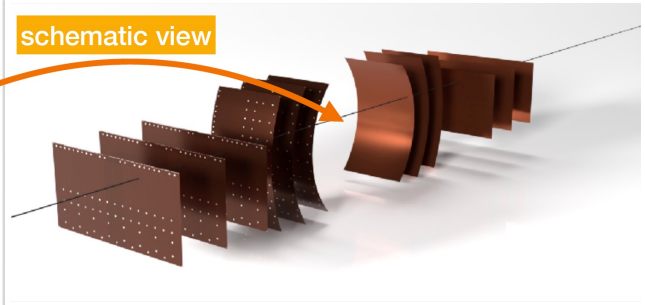
- **Test beam with full mock-up of the final ITS (“μITS3”) in Jul 2021 (SPS)**
  - **6 ALPIDE chips bent to the target radii of ITS3**
  - **Cu target in the center ➔proton/pion-Cu collisions**
  - **Track and vertex reconstruction**







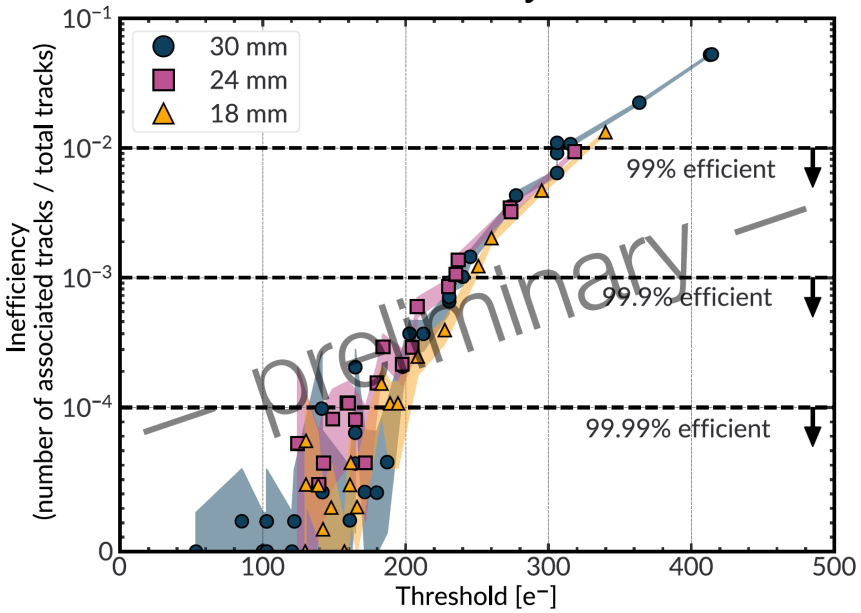




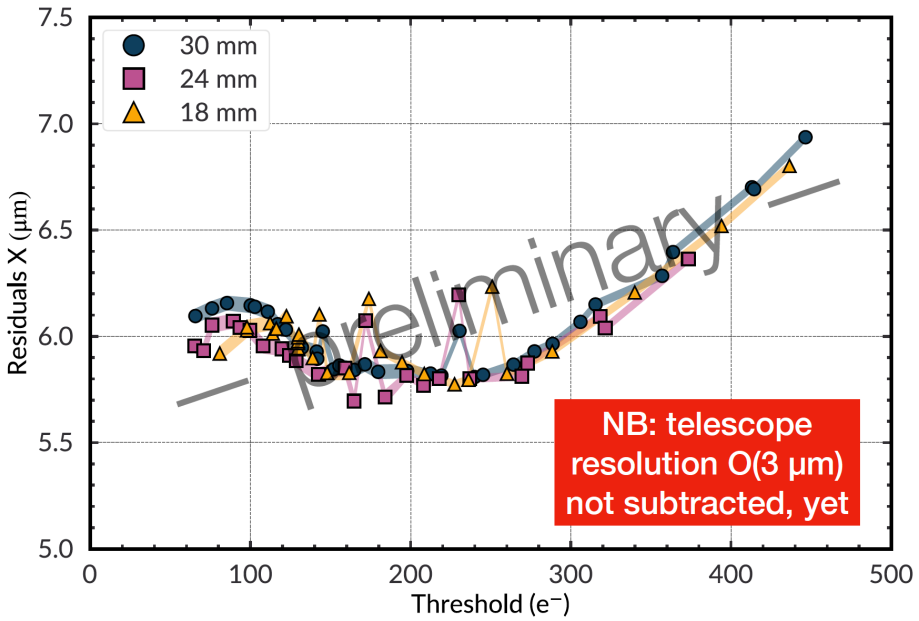
- **Test beam with full mock-up of the final ITS ("μITS3") in Jul 2021 (SPS)**

- **Consistent performance for bent chips of different radii**

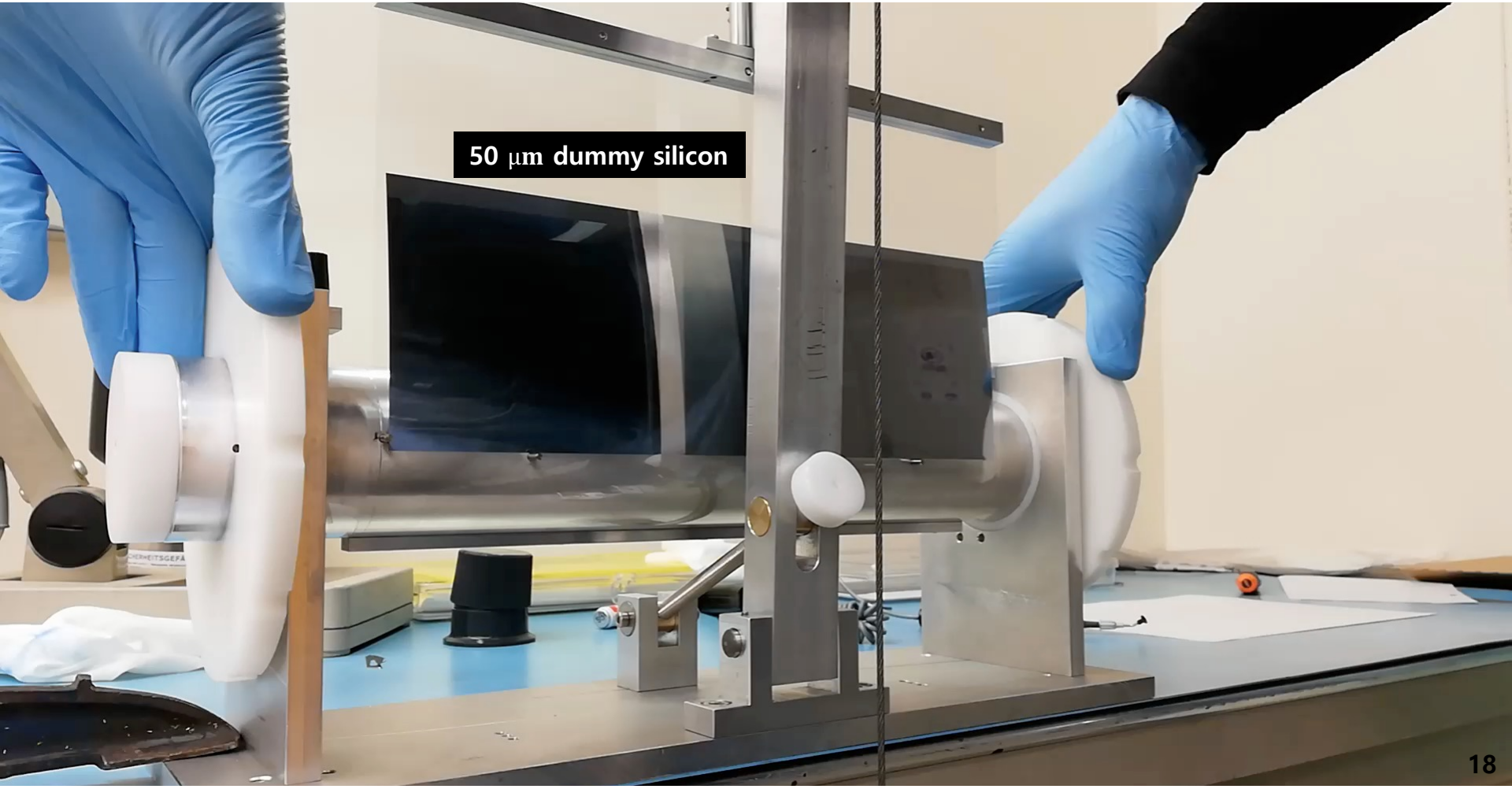
Efficiency



Residual

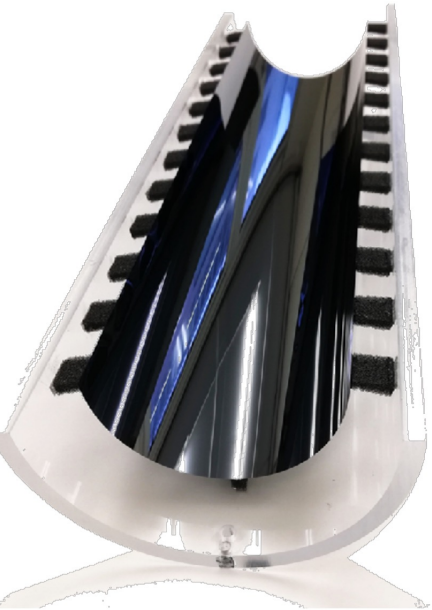


Bending wafer-scale sensors

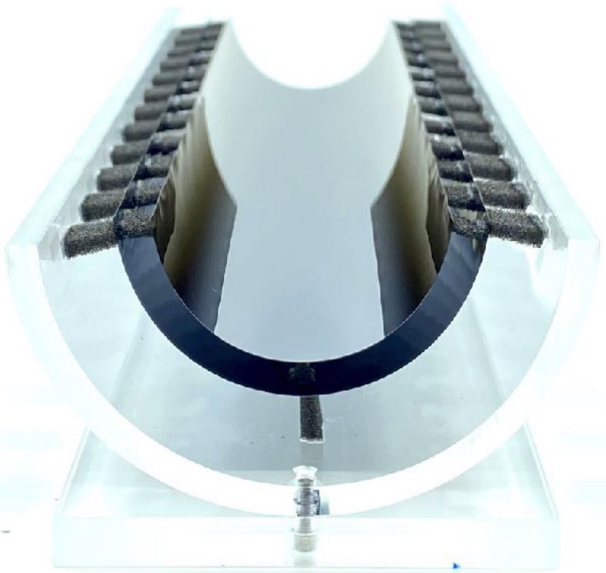


- **Successfully integrated 3 silicon layers**

Layer 2

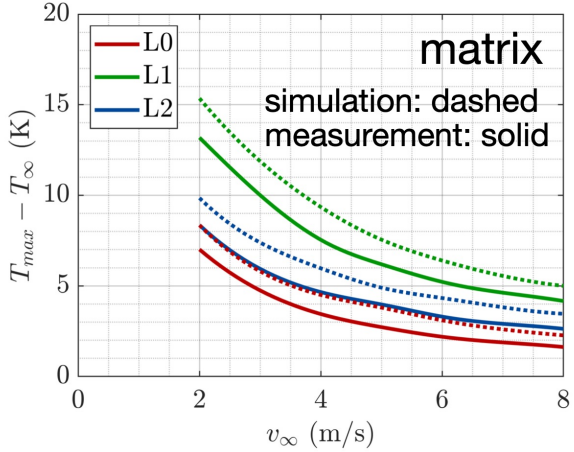


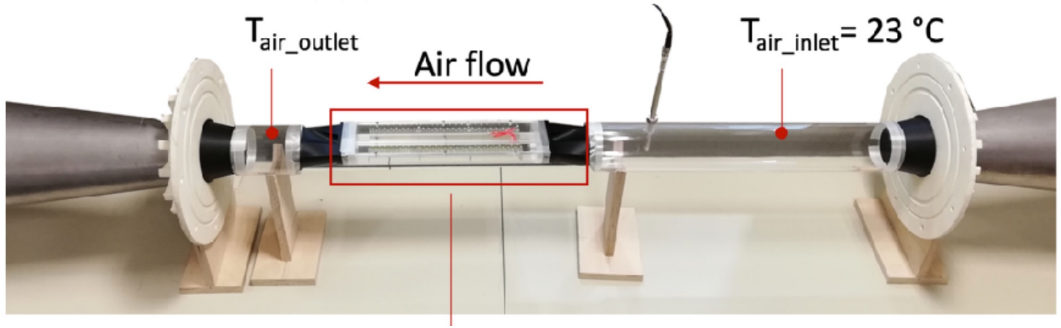
Layers 2+1

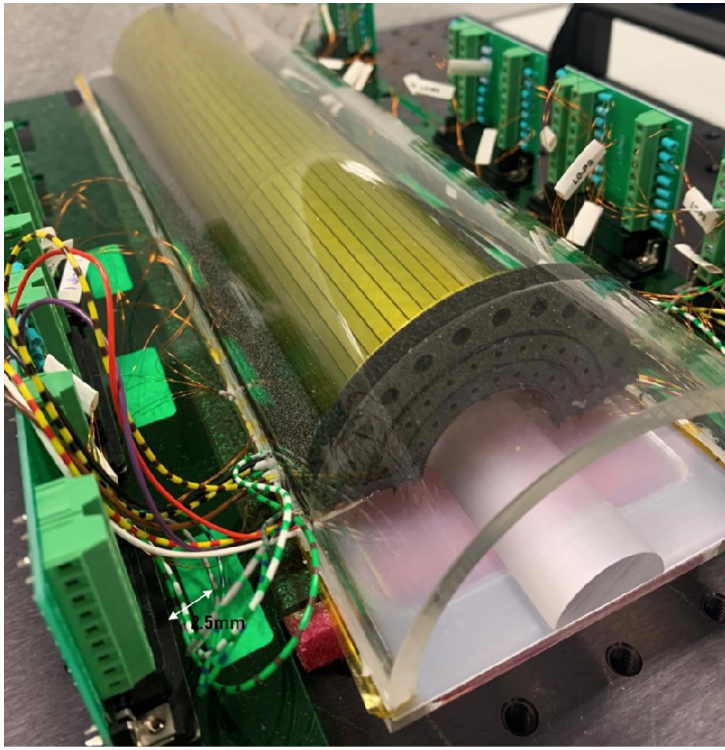


Layers 2+1+0

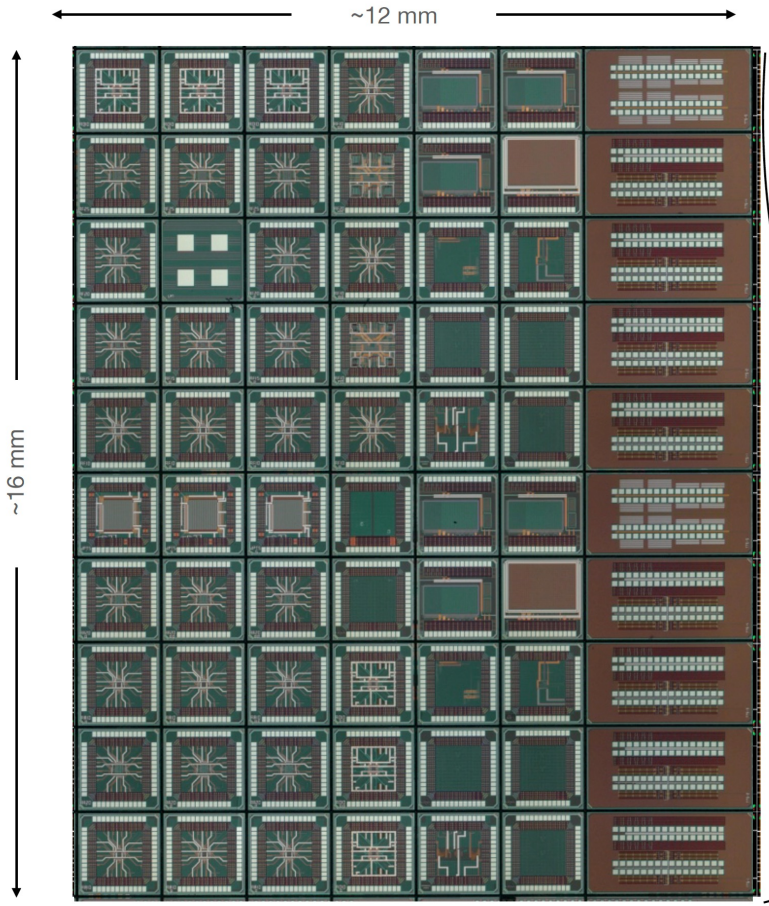
- **Preliminary test for cooling system**
  - **Breadboard models based on heating elements**
  - **Study of thermal properties in a wind tunnel**



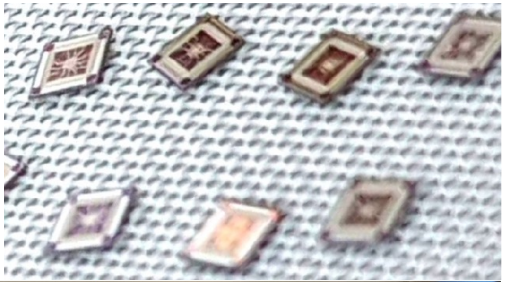


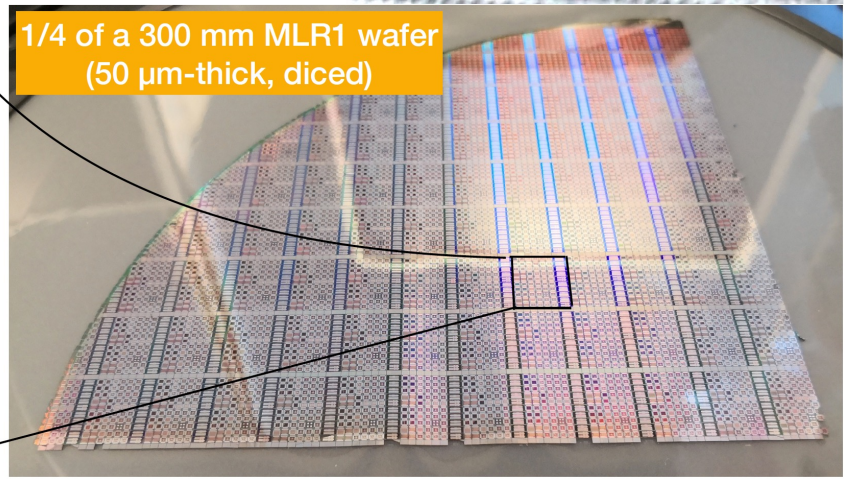


Sensor development with the 65 nm process



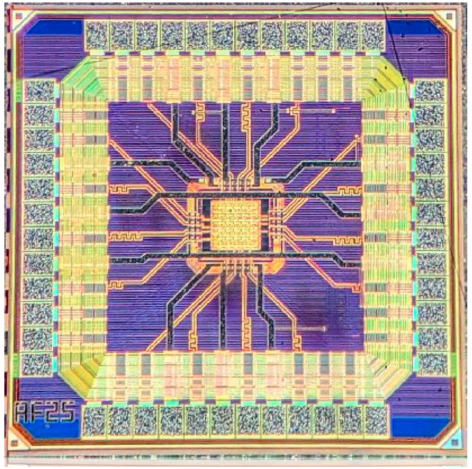
- **First submission with test chips (2021 summer)**
  - **Transistors, DACs, analog pixels, digital pixels**
- **Several tests are ongoing**





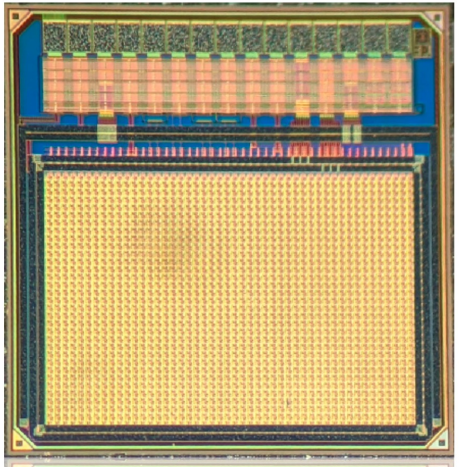
Sensor development with the 65 nm process

APTS



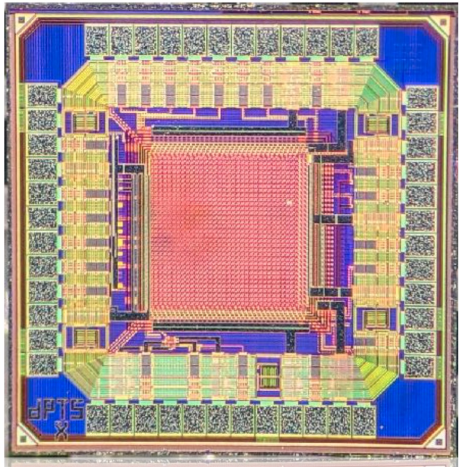
- Matrix: 6x6 pixels
- Readout: direct analog readout of central 4x4
- Pitch: 10, 15, 20, 25 μm

CE65



- Matrix: 64x32, 48x32 pixels
- Readout: rolling shutter analog
- Pitch: 15, 25 μm

DPTS



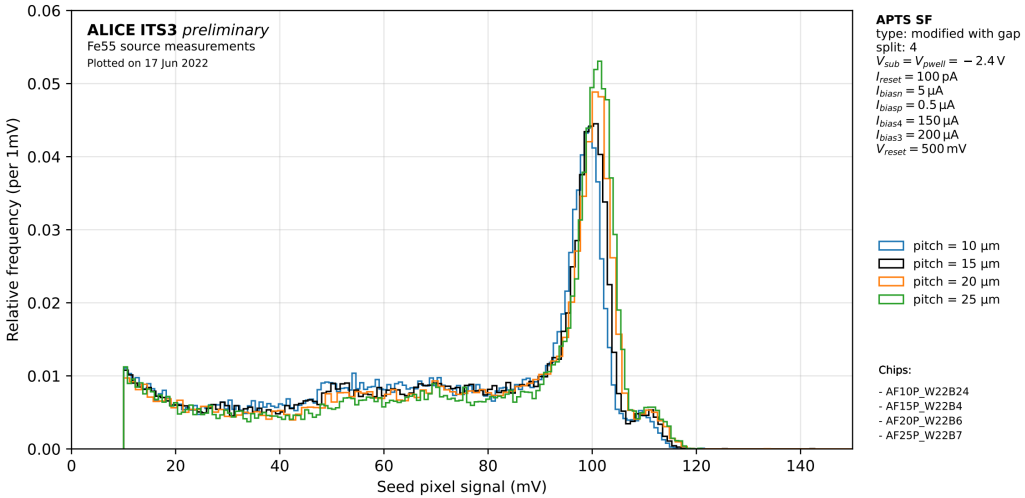
- Matrix: 32x32 pixels
- Readout: asynchronous digital readout
- Pitch: 15 μm

APTS – Lab test with Fe-55

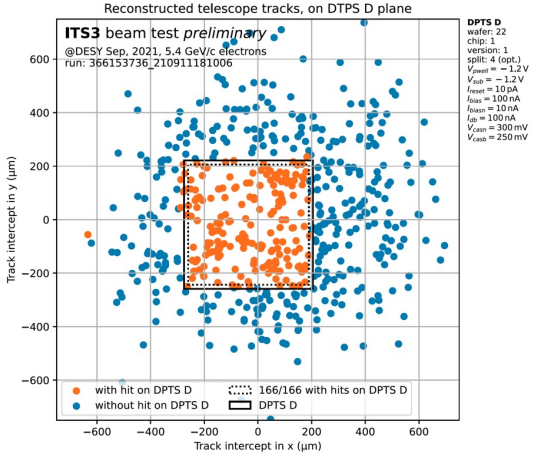
- **Comparison of various pixel pitches to study the optimal pitch**

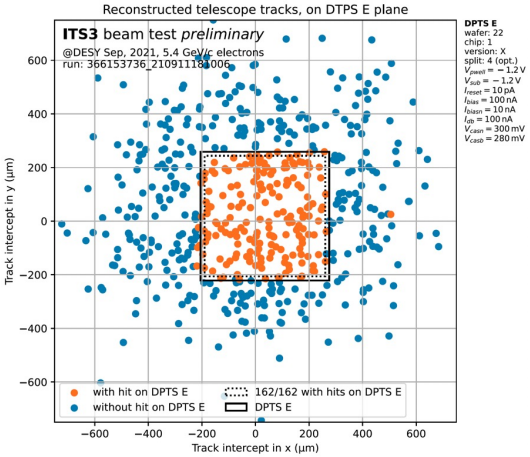
- **Modification in the process**
  - **Full depletion of sensors**
  - **Electric field pointing to collection electrodes**

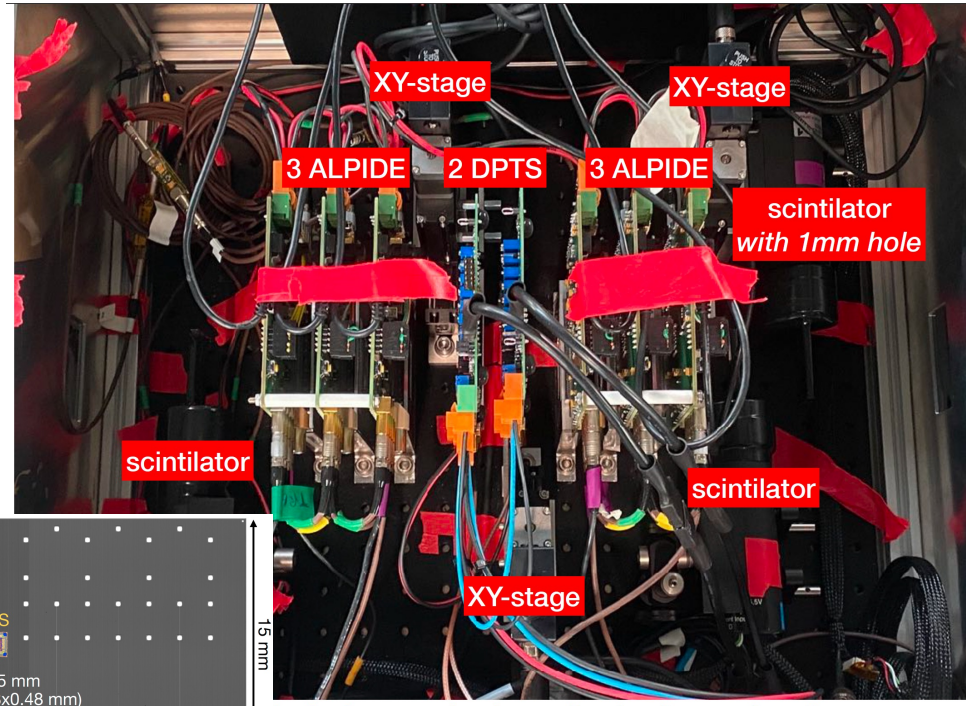
- **Similar results between pixels of different pitches (10-25 μm)**
  ➔Very efficient charge collection

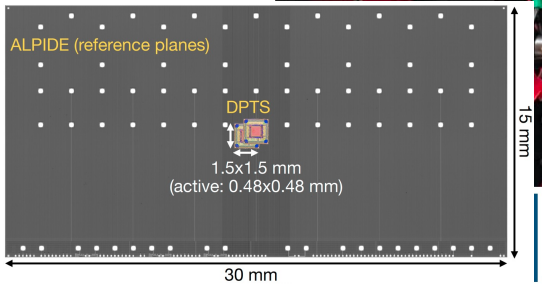


- **100% detection efficiency from the first data**



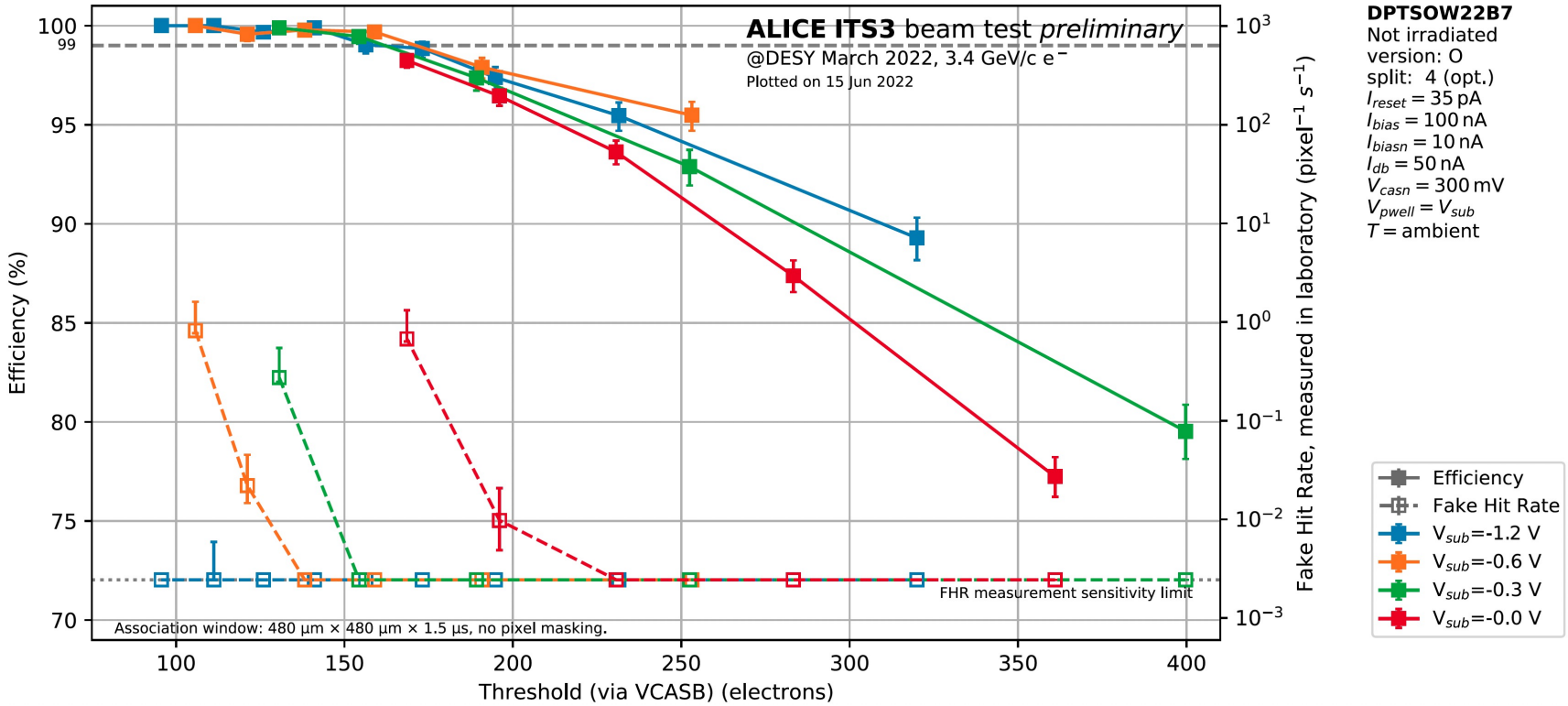






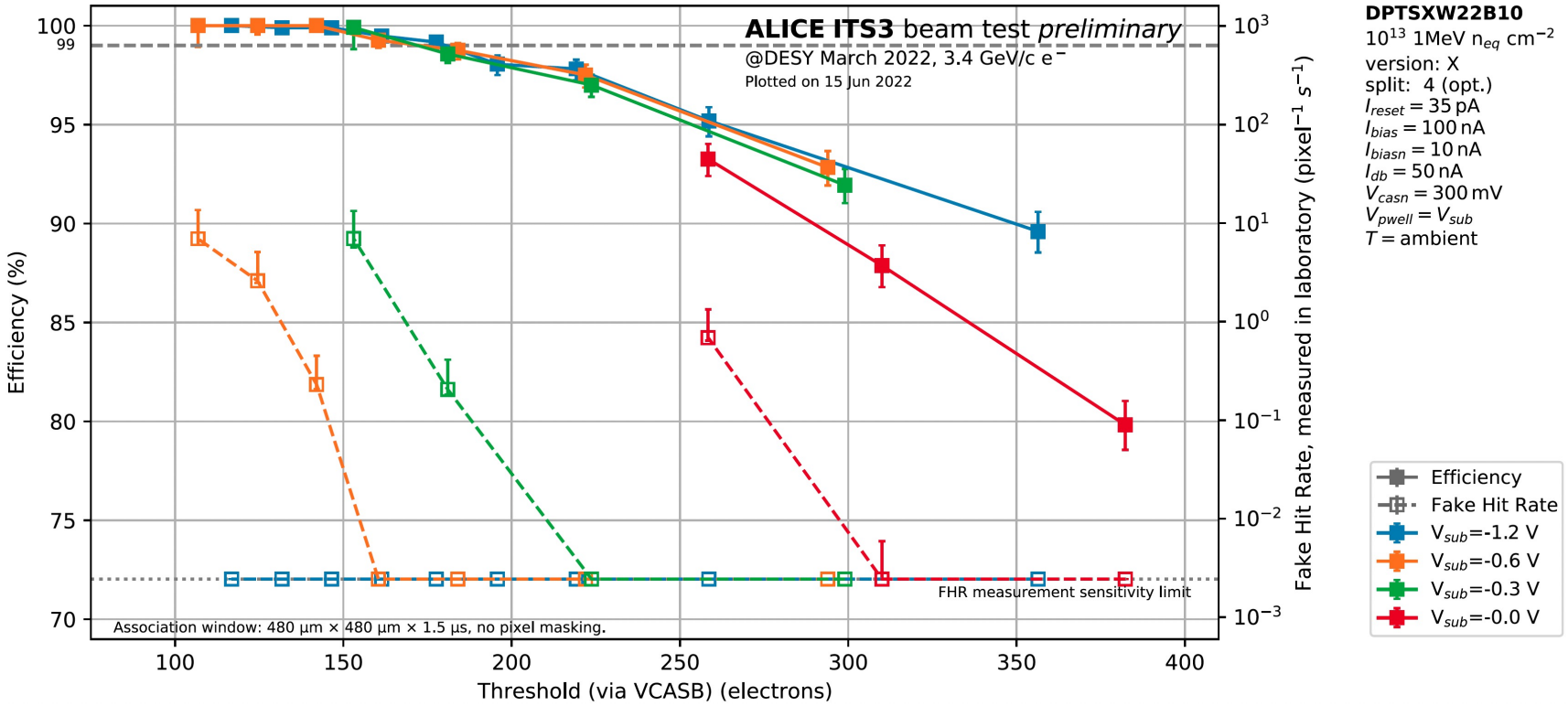
- **Efficiency and fake hit rates**

➔Excellent detection efficiency at very low fake hit rates over a large threshold range

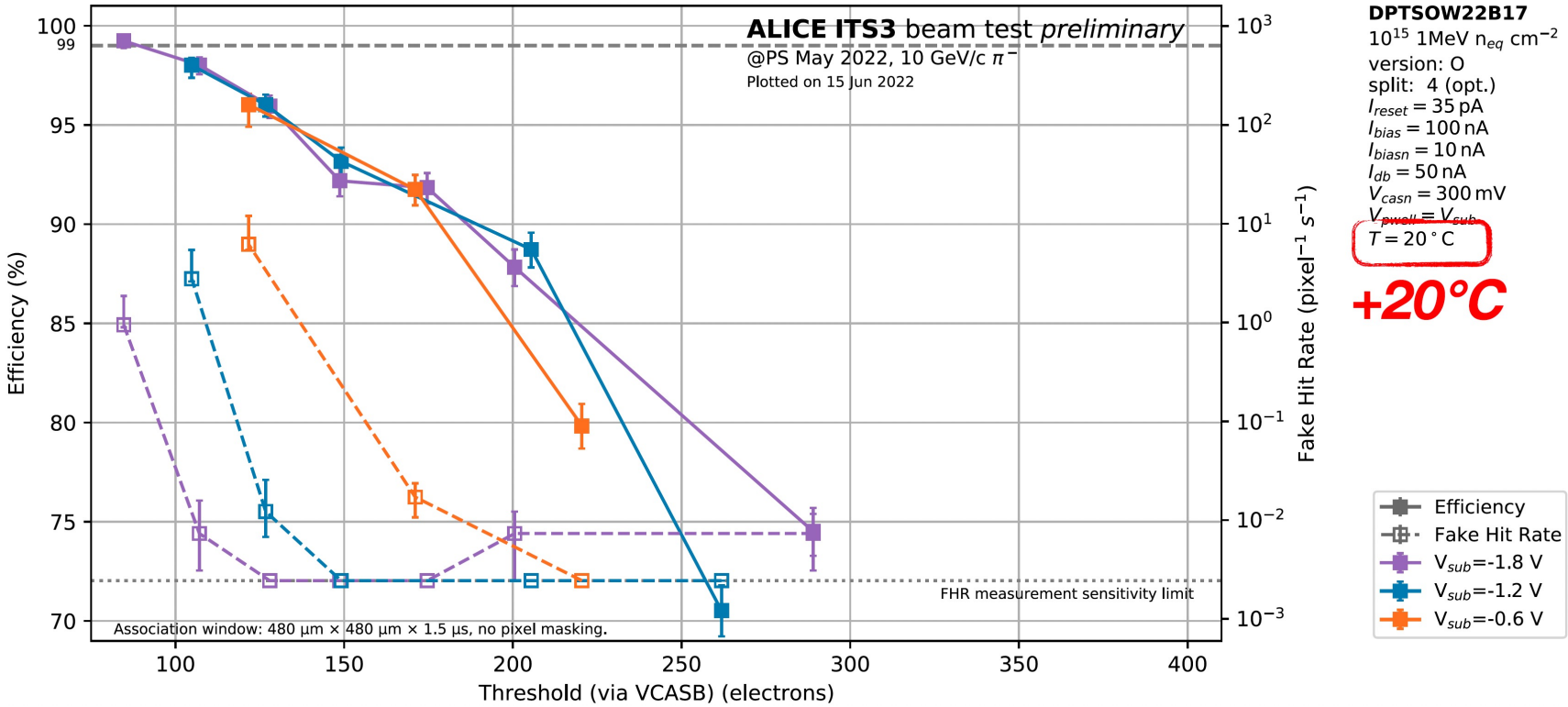


- **After irradiation: 10^{13} NIEL**

  ➔At ALICE conditions: still high detection efficiency with slightly larger fake rates

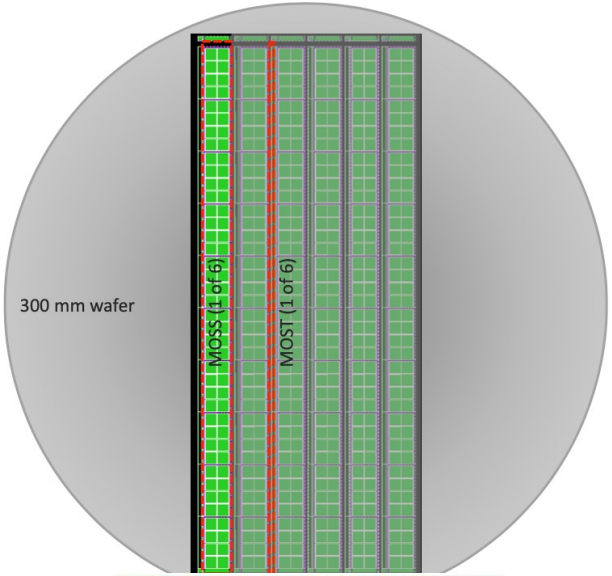


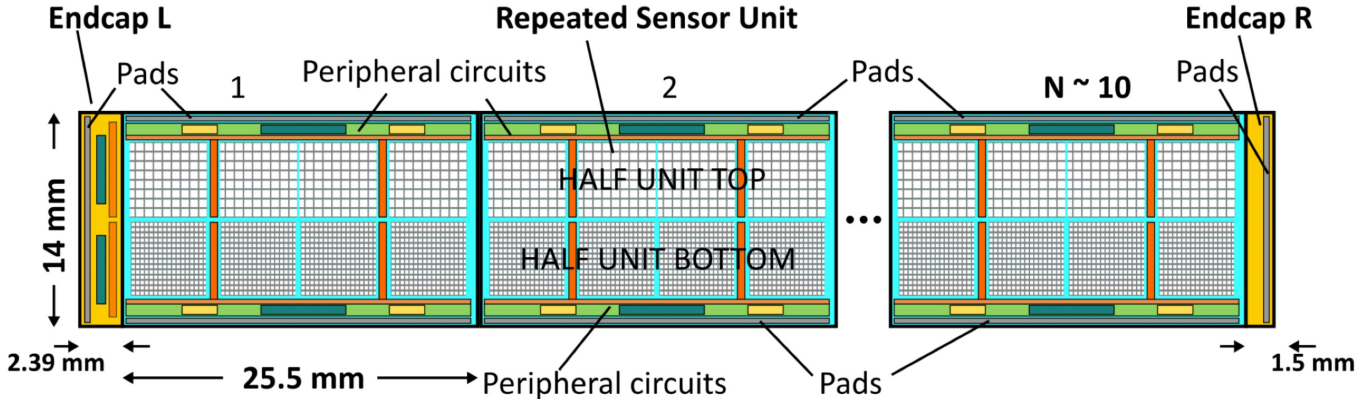
- **After irradiation: 10^{15} NIEL**
  ➔Still possible to achieve high efficiency at room temperature

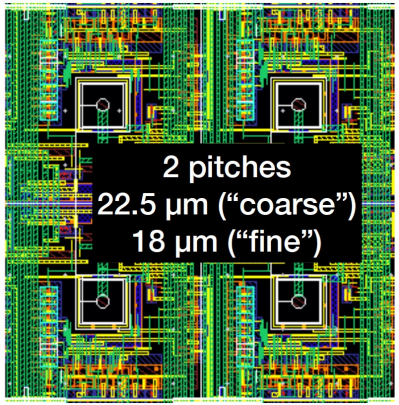


Wafer-scale sensors with stitching

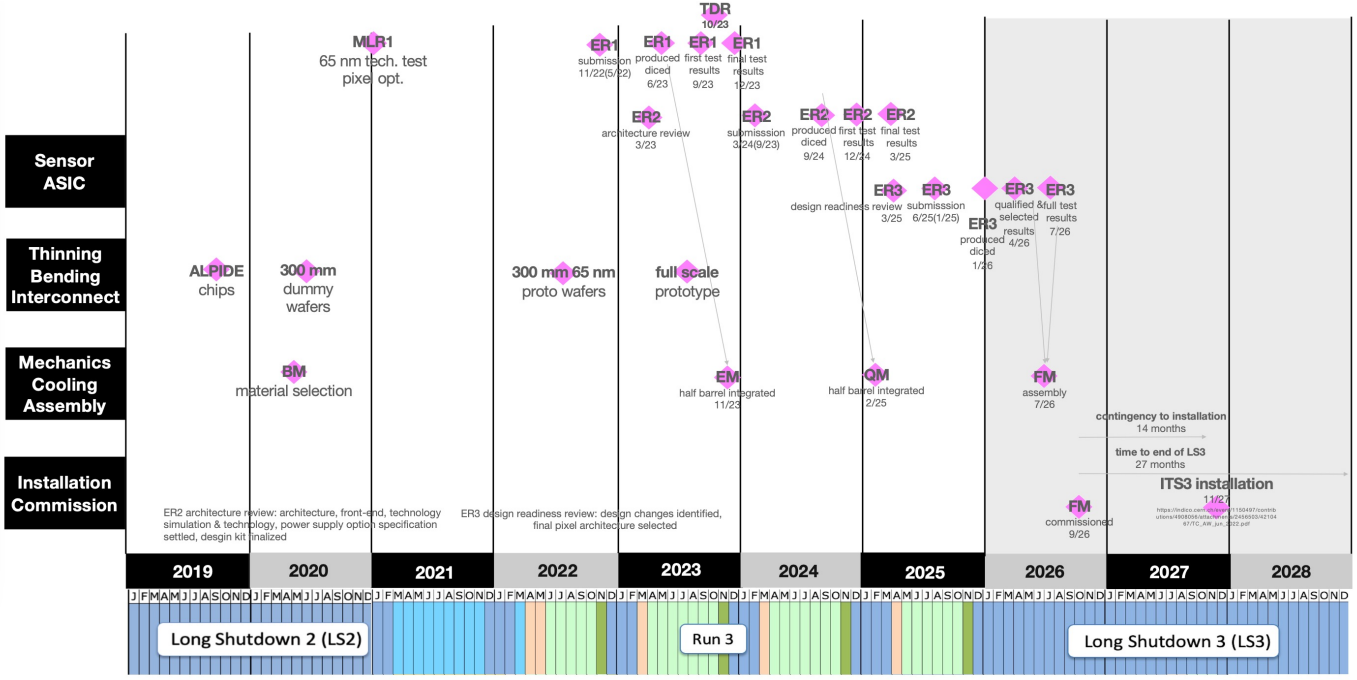
- **Engineering run for prototype sensors is prepared**
  - **Expect sensors for testing at mid-2023**
  - **Yield from the stitching technique**
  - **Interconnect power and signals**
  - **Study of noise, speed, leakage…**
- **Preparation for post-processing and testing is ongoing**







- **Active R&D is ongoing in ALICE for a new inner tracking system (ITS3) for LHC LS3**
  - **Wafer-scale sensors with stitching (65 nm process)**
  - **Very low material budget (<0.05% X_0 per layer)**
  - **Initial performance has been done for bent chips with ALPIDE and test chips from MLR1**



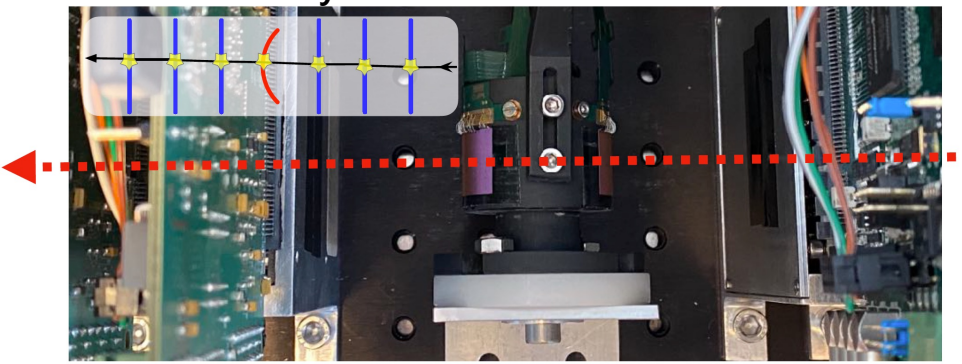
MLR: multiple layer per reticle, **ER:** engineering run (6 months turn-around),
BM: breadboard module, **EM:** engineering module, **QM:** qualification module, **FM:** final module

planning uncertainty:
ASIC design using new technology without established design work flow, ASIC design is in R&D mode → large chip implementation and electro-mechanical implementation depends on findings during R&D

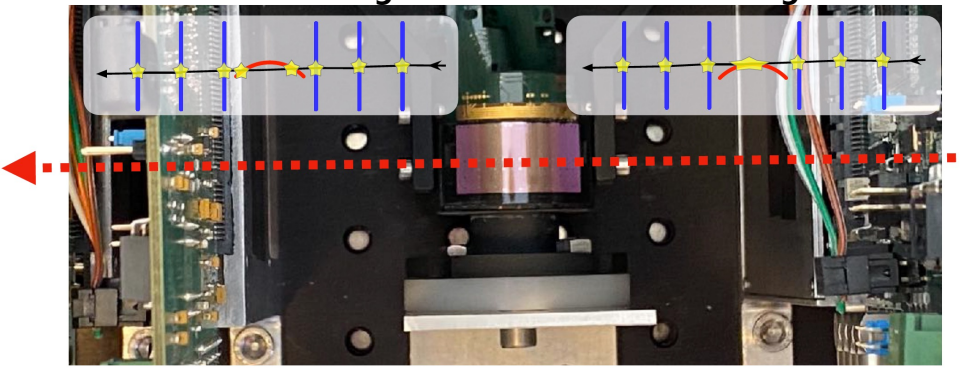
BACKUP

- **Test with different geometries**

Ordinary



Double-crossing **Grazing**



hitmap