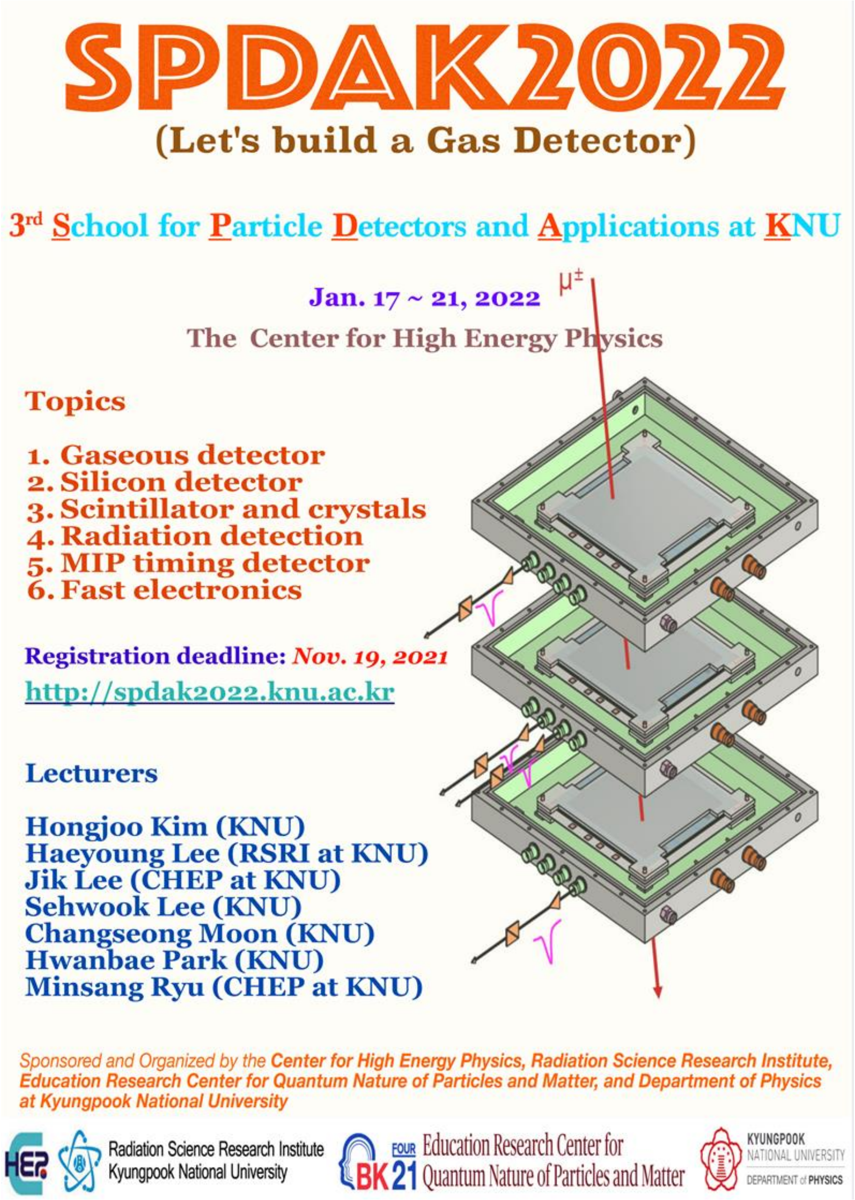
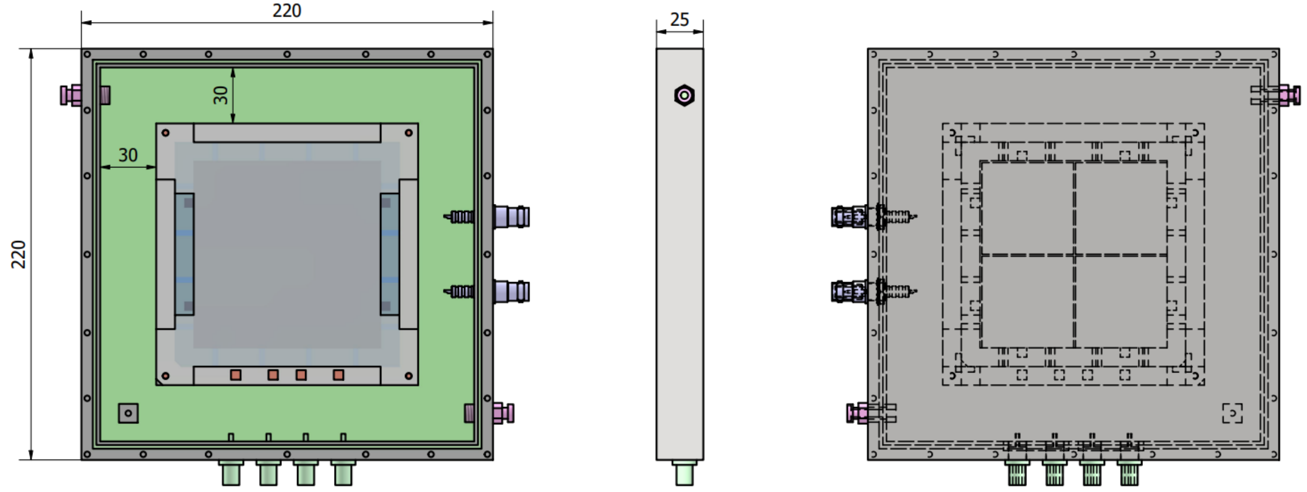


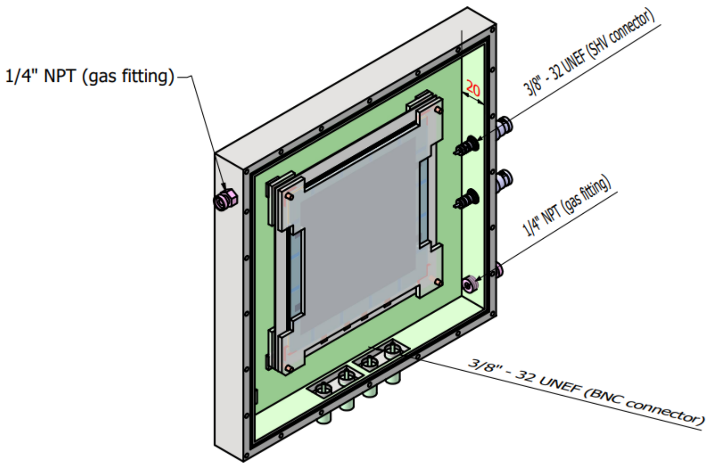
Resistive Plate Chamber
:construction and test

RYU, Min Sang

CHEP at KNU

Gas vessel of RPC

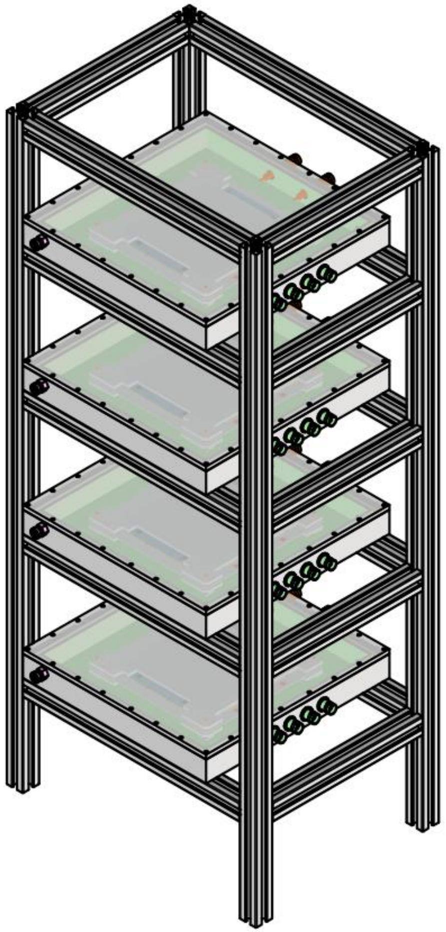




- Gas volume of RPC
  - inner volume: 0.8 L (200x200x20 mm^3)

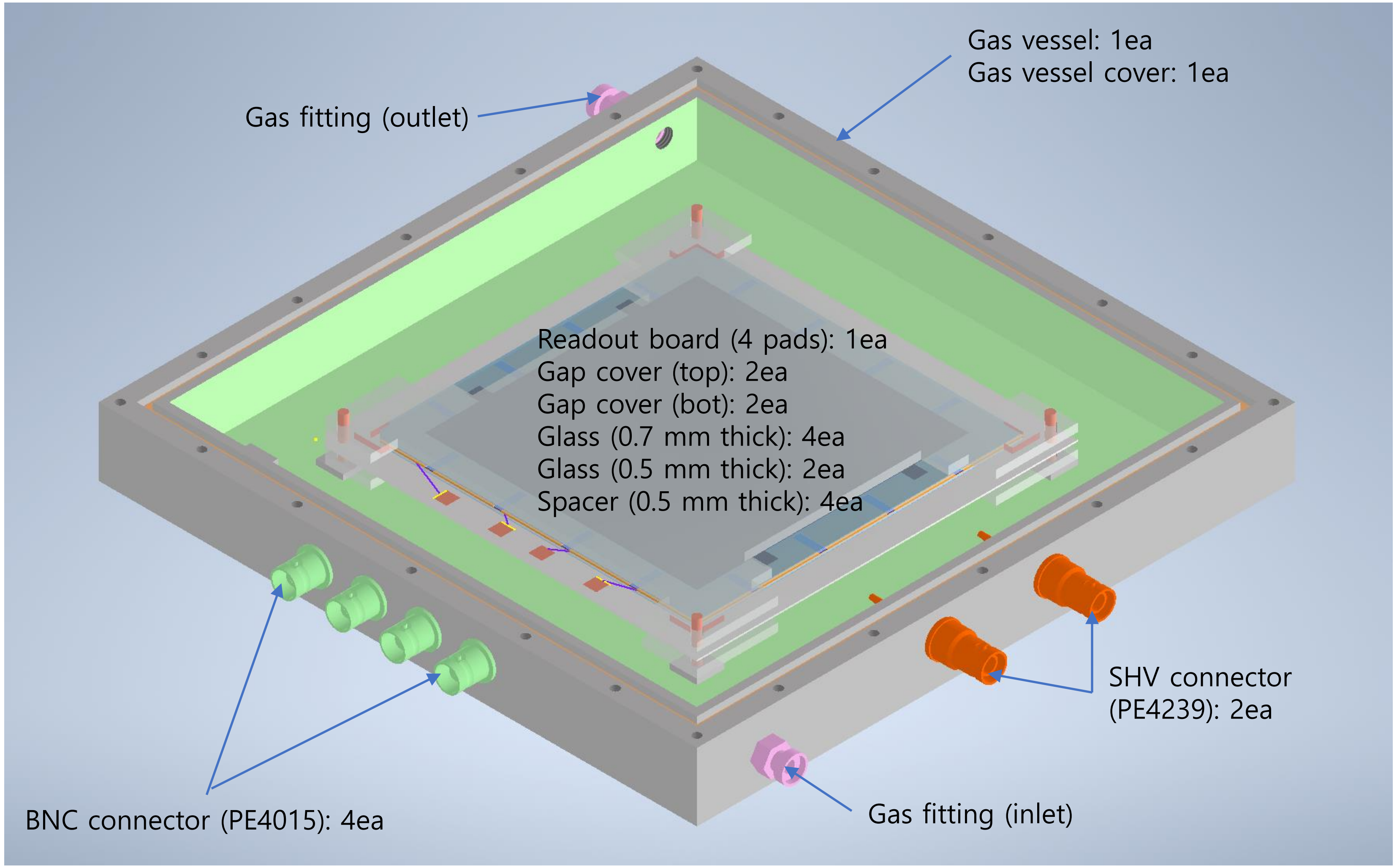
- Gas flow rate
  - Flushing: 60 cc/min (3.6 L/h) ➔ 4.5 times/h
  - Operation: 20 cc/min (1.2 L/h) ➔ 1.5 times/h

Cosmic-ray Test Stand



Test gas: Ar : O_2 : i-C_4H_{10} : CO_2 = 30 : 5 : 6 : 59%

Main components of Multi-gap Glass RPC



Multi-gap Glass RPC
Gas vessel: 1ea
Gas vessel cover: 1ea

SHV connector (PE4239): 2ea
BNC connector (PE4015): 4ea
Gas fitting: 2ea

Gap configuration: 4 gaps (2 + 2)
Glass (0.7 mm thick): 4ea
Glass (0.5 mm thick): 2ea
Spacer (0.5 mm thick): 4ea

Readout board (4 pads): 1ea
Gap cover (top & bottom): 2ea

Assembly the connectors of Multi-gap Glass RPC

Connector 부착

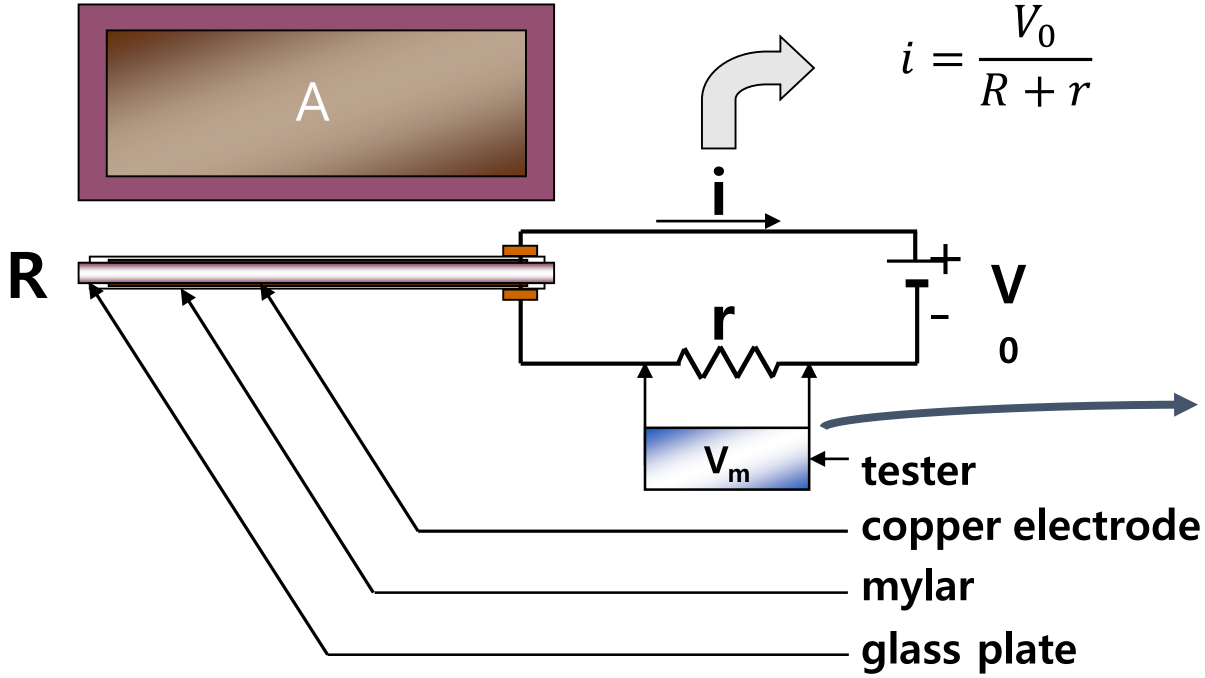
Epoxy (5 min)

Connector 부착 완료

Bulk resistivity of resistive plate

$$R = \rho \frac{d}{A}$$

ρ: bulk resistivity
A: area of the electrode
d: thickness of glass plate



$$i = \frac{V_0}{R + r}$$

$$V_m = i \times r$$

$$i = \frac{V_0}{R+r} = \frac{V_m}{r}$$

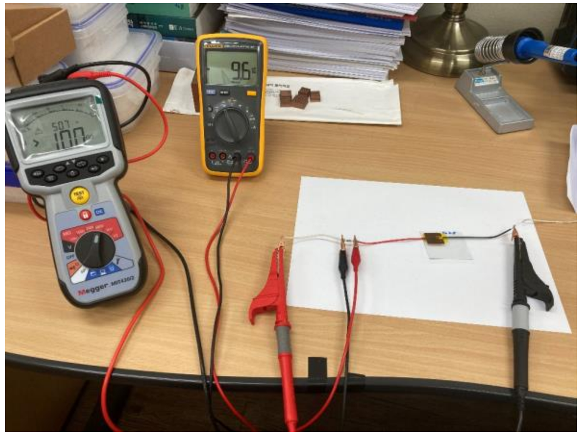
➔ $R = r\left(\frac{V_0}{V_m} - 1\right)$

➔ $\rho = \frac{Ar}{d}\left(\frac{V_0}{V_m} - 1\right)$

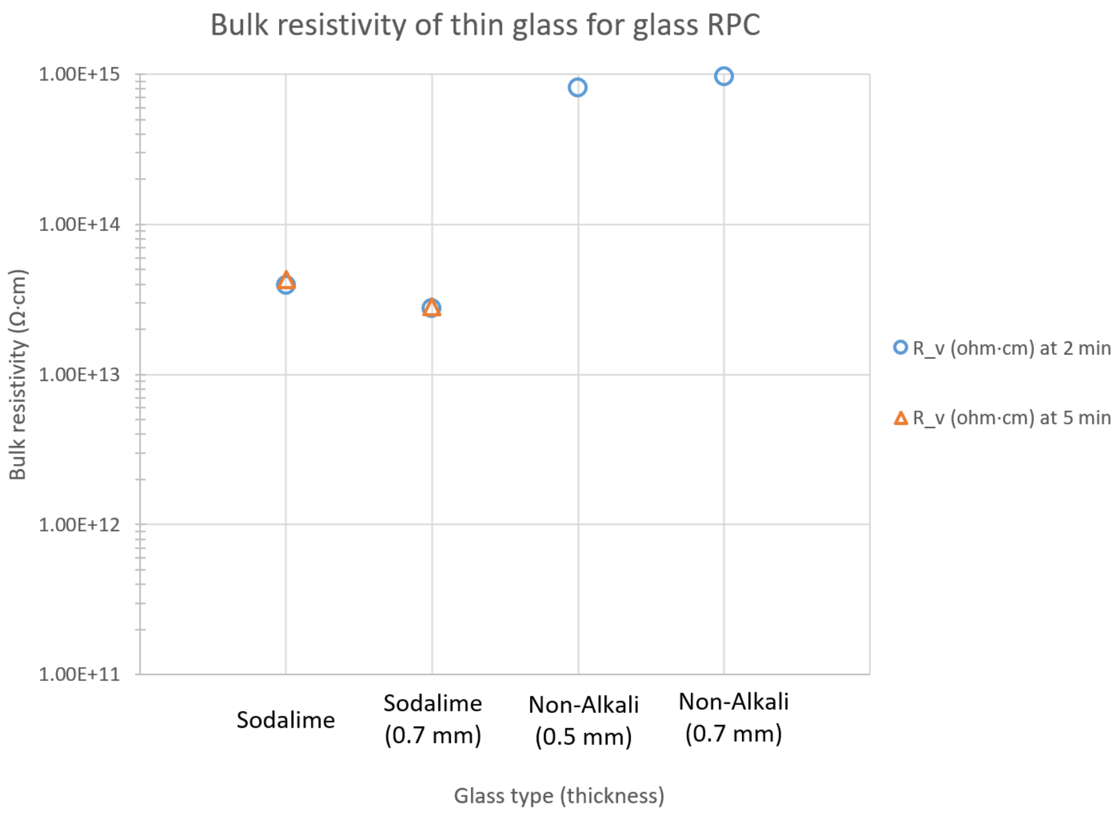
Bulk resistivity of resistive plate

$$\rho = \frac{Ar}{d}\left(\frac{V_0}{V_m} - 1\right)$$

ρ: bulk resistivity
A: area of the electrode
d: thickness of glass plate



0.5 mm glass (S.L.)



Voltage measurement (5 min)

0.5 mm glass: V_m = 9.6 mV at V_0 = 507 V

$$\rho = \frac{Ar}{d}\left(\frac{V_0}{V_m} - 1\right) = \frac{(2 \times 2)cm^2 \ 10\ M\Omega}{0.05\ cm}\left(\frac{507\ V}{9.6\ mV} - 1\right) = {\sim}4.2 \times 10^{13}\Omega \cdot cm$$

0.7 mm glass: V_m = 10.3 mV at V_0 = 507 V

$$\rho = \frac{Ar}{d}\left(\frac{V_0}{V_m} - 1\right) = \frac{(2 \times 2)cm^2 \ 10\ M\Omega}{0.07\ cm}\left(\frac{507\ V}{10.3\ mV} - 1\right) = {\sim}2.8 \times 10^{13}\Omega \cdot cm$$

Voltage drop and time constant with bulk resistivity

Time constant

$$\tau = R \cdot C = \rho\left(\frac{d}{A}\right) \times \varepsilon_0\left(\frac{S}{l}\right) = \rho \cdot \varepsilon_0\left(\frac{d}{l}\right)$$

- ρ: bulk resistivity of resistive plate
- A and S: active areas of electrode
- l: total gap thickness
- d: total thickness of resistive plate
- $\varepsilon_0 = 8.845 \times 10^{-12}\ \mathrm{F \cdot m^{-1}}$

$$\tau = 4 \times 10^{11}(\Omega \cdot m) \times 8.845 \times 10^{-12}(F \cdot m^{-1})\left(\frac{0.05 + 2 \times 0.07\ (cm)}{2 \times 0.05\ (cm)}\right) = 672\ \mathrm{ms}$$

➔ Low rate capability due to increasing recovery time by high bulk resistivity

Voltage drop

$$V_d = 2 < Q_e > \rho \cdot r \cdot d_0$$

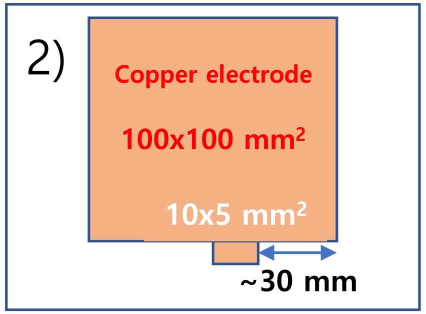
- $< Q_e >$: integrated mean charge
- ρ: bulk resistivity of resistive plate
- r: incident particle rate ($\mathrm{Hz/cm^2}$)
- d_0: total thickness of resistive plate

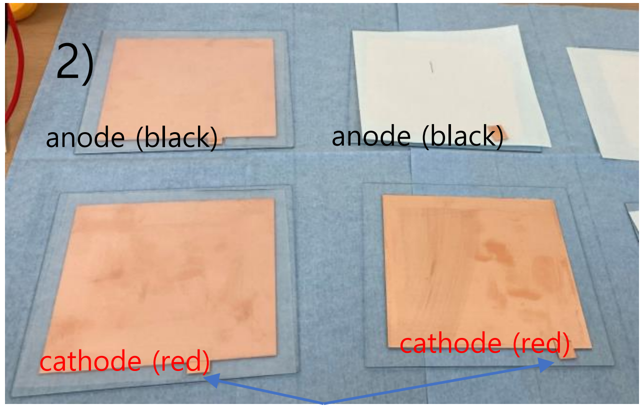
$$V_d = 2 \times 1(pC) \times 4 \times 10^{13}(\Omega \cdot cm) \cdot 20\left(\frac{Hz}{cm^2}\right) \times (0.05 + 2 \times 0.07\ (cm)) = 304\ \mathrm{V}$$

➔ Low rate capability due to increasing inefficient while particle rate increases

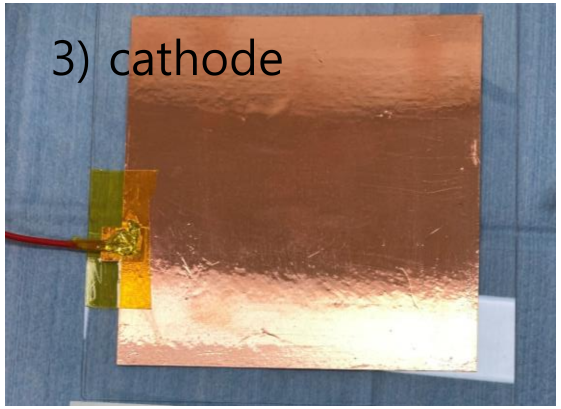
Assembly the electrode on the resistive plate

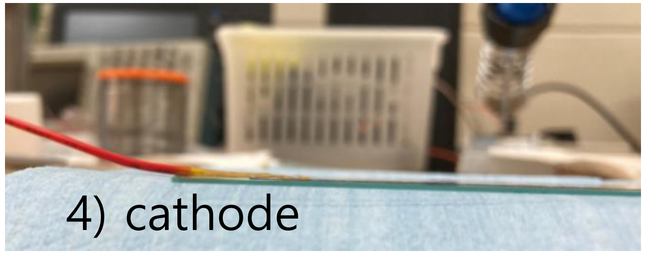
1) All the edge of glasses and spacers should be polished by sand paper.
2) Attach the copper tape (100x100 mm^2) on the glass (0.7 mm thick)
3) Solder the cable on the copper electrode: cathode (red), anode (black), signal (white)
4) Measure the thickness of soldering area
5) Glue the few insulation sheets (each thickness is ~0.2 mm)

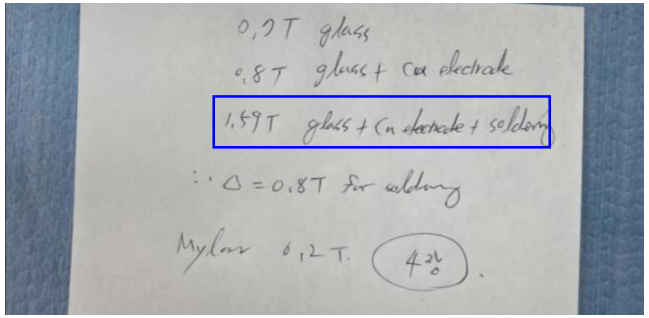


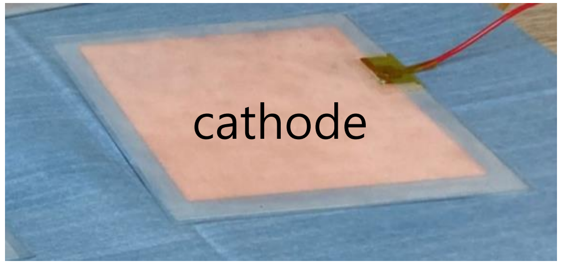


Soldering point of cables

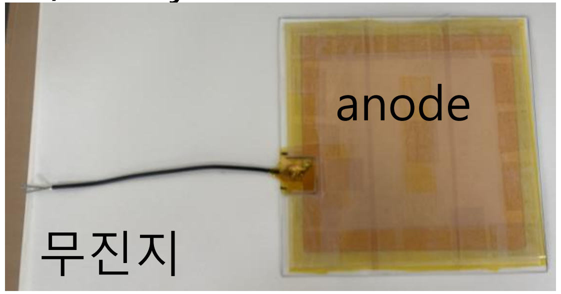




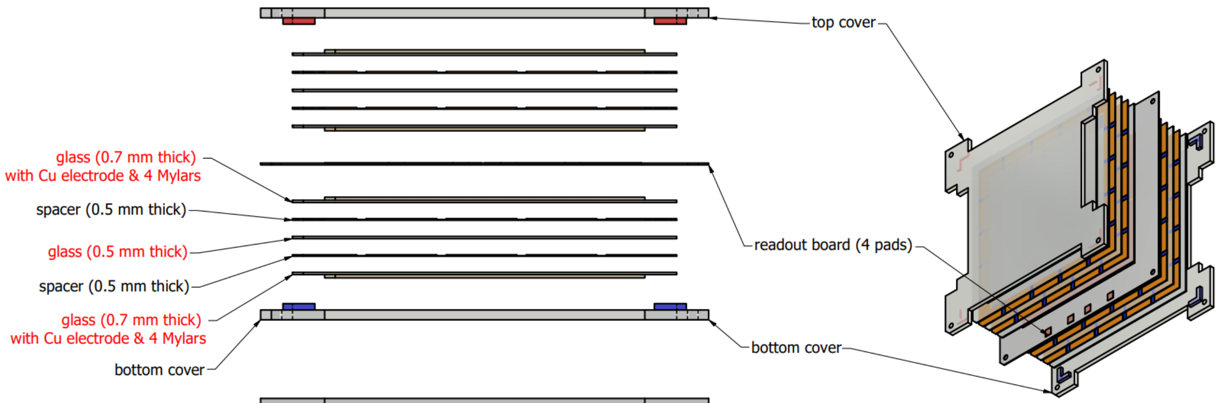


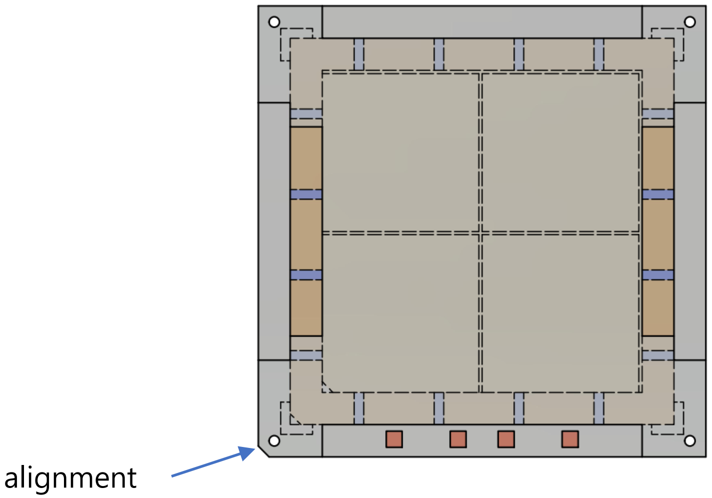


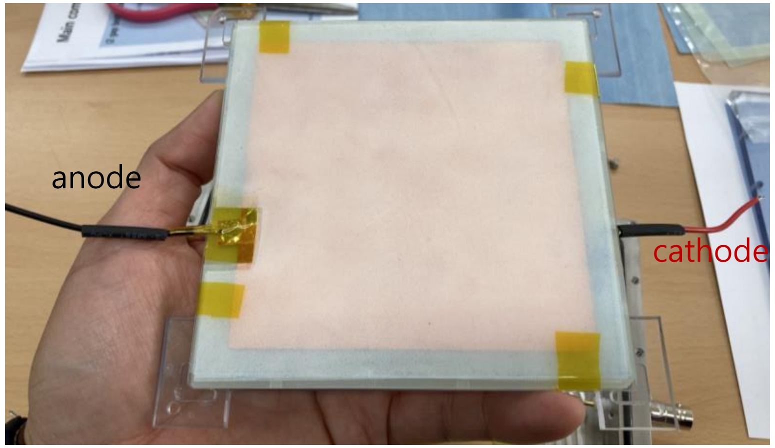
5) 4 mylar sheets



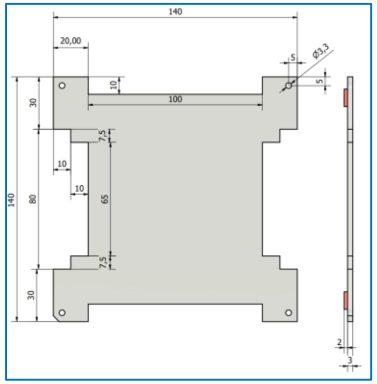
How to stack 4 Gap Configuration?



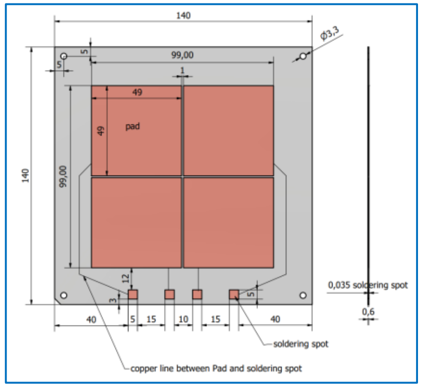




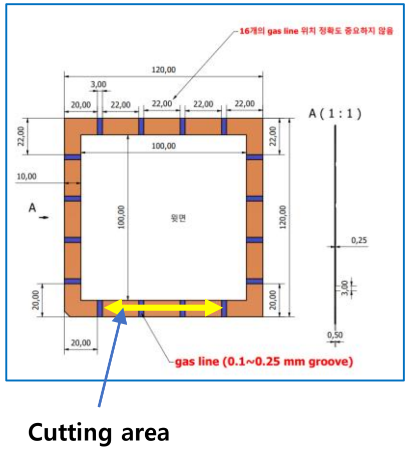
Top & Bottom cover



Readout board (4 pads)

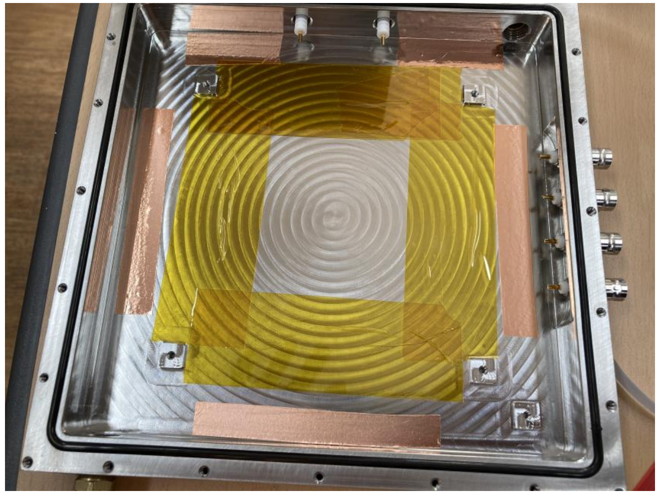


Spacer (0.5 mm thick)



How to assemble the 4 gap glass RPC?

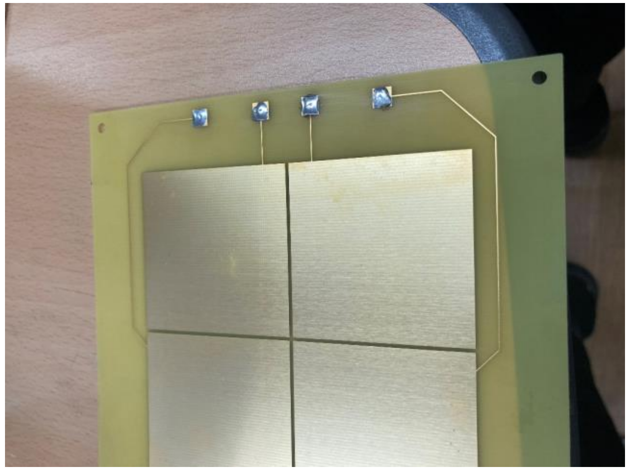
1) Insulation sheet near HV connectors



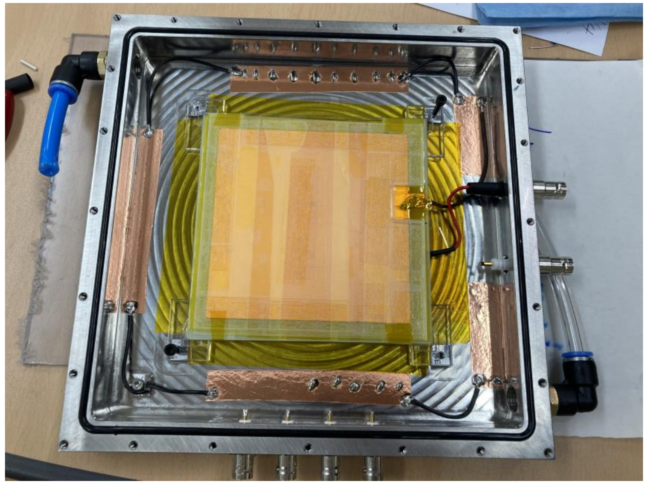
2) Soldering preparation

3) Cable soldering on BNC connectors and GND spot

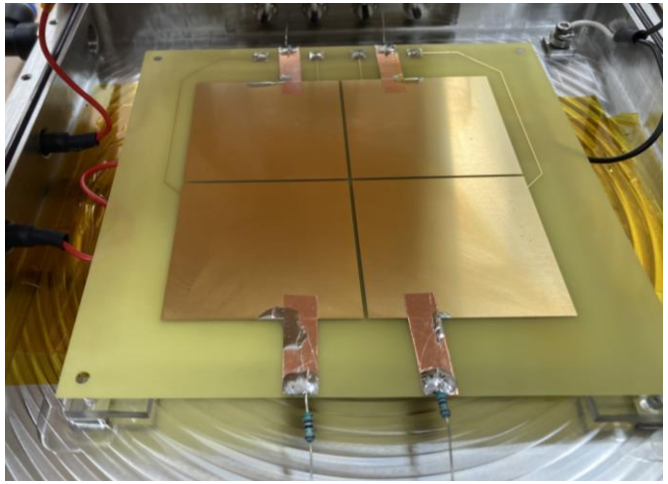
4) Soldering preparation on readout board



5) Mounting bottom gap

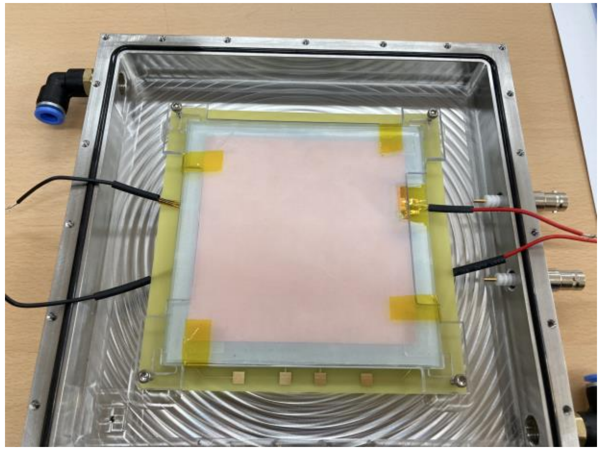


6) Mounting readout board (50 ohm)

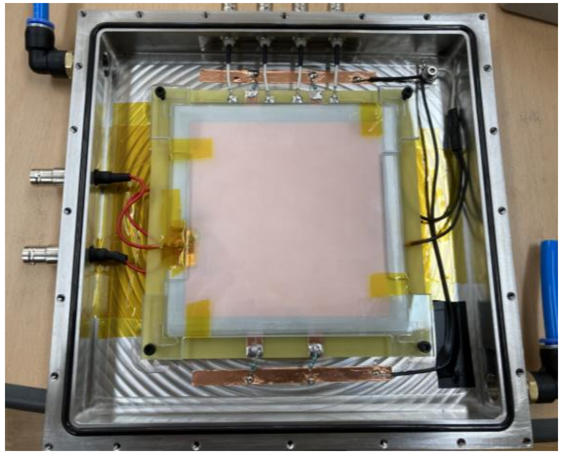


How to assemble the 4 gap glass RPC?

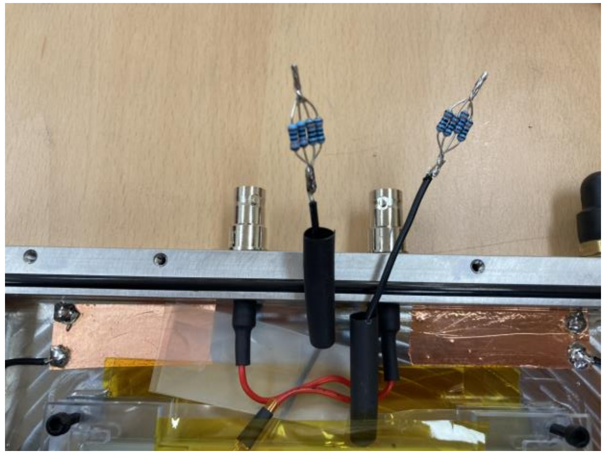
7) Mounting top gap

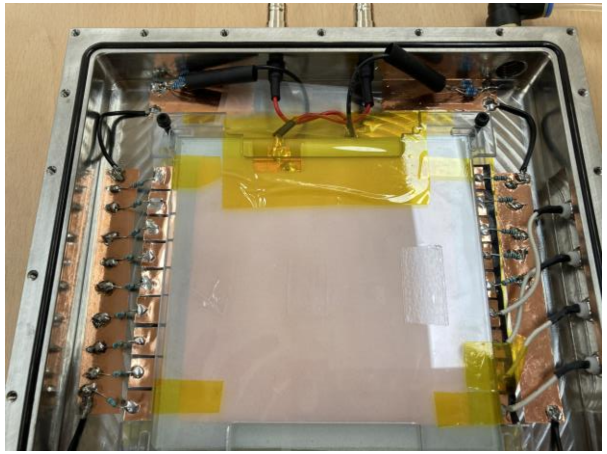


8) Soldering all cables

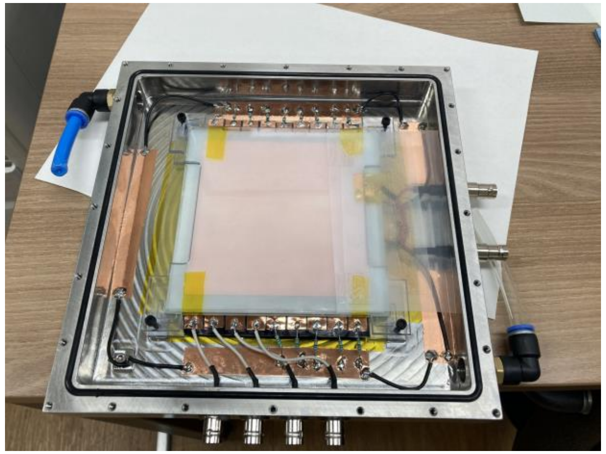


9) Connection 100 kohm with GND electrodes

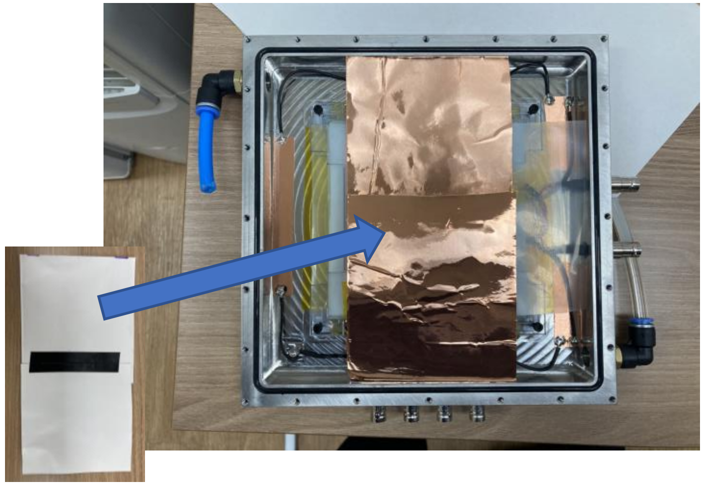




9) Attach the insulation sheet near HV connection



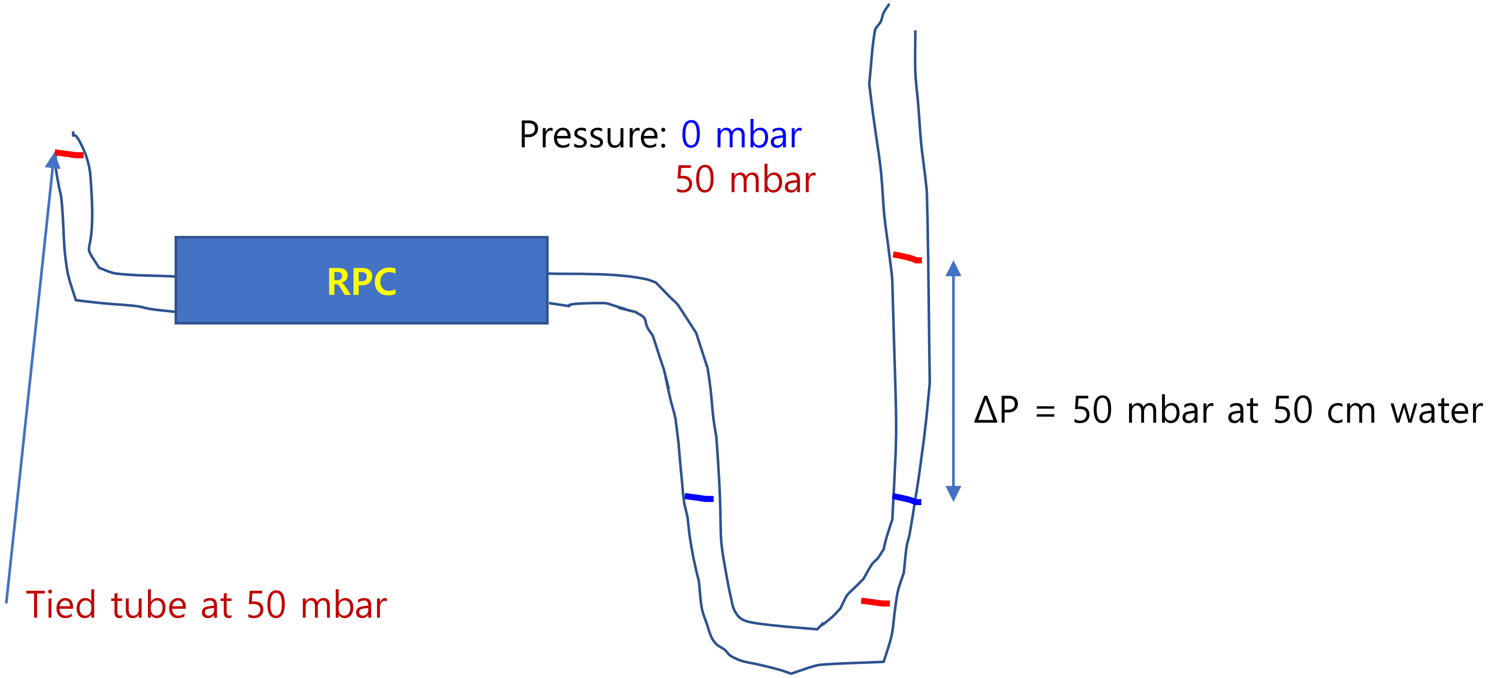
10) Attach the copper sheet on the top cover

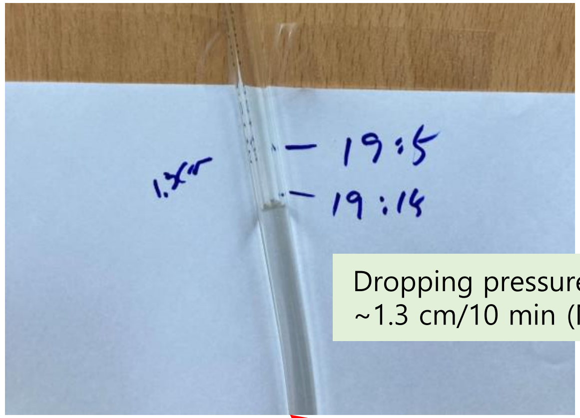


Gas leakage test

11) Sealing the chamber

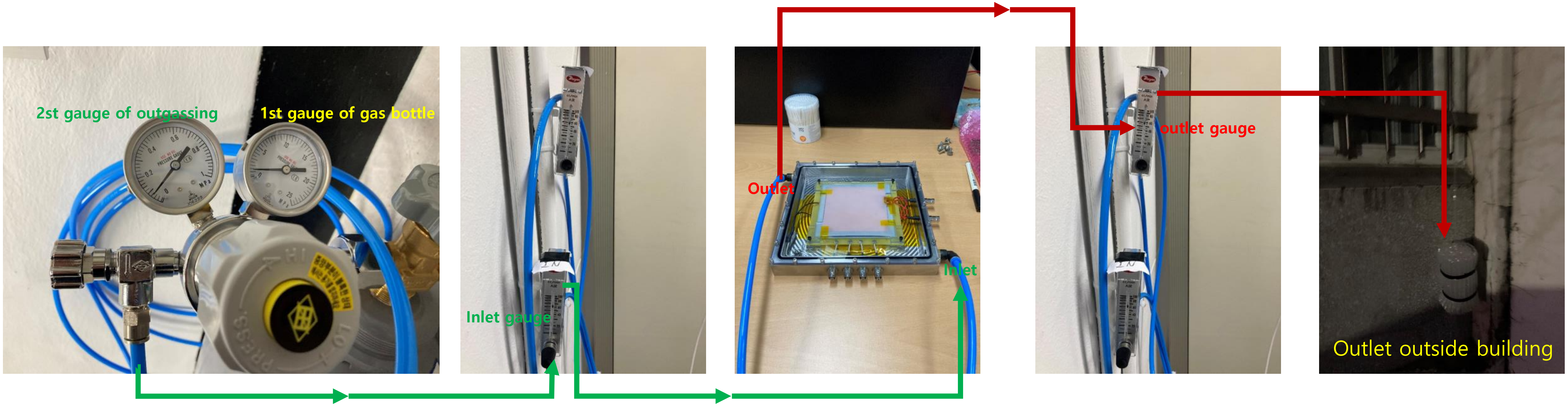
12) Gas leakage test



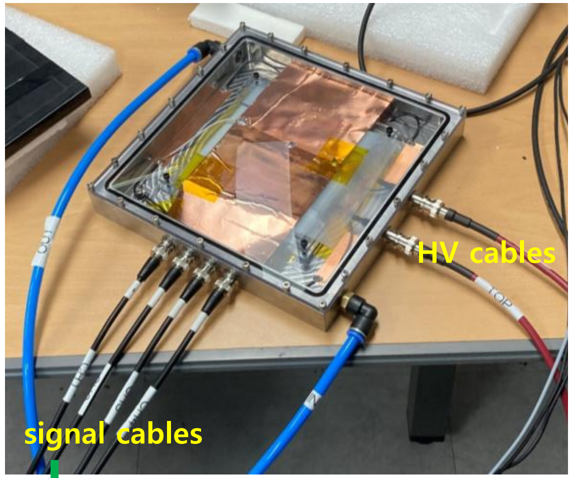


Dropping pressure rate
~1.3 cm/10 min (Not perfect)

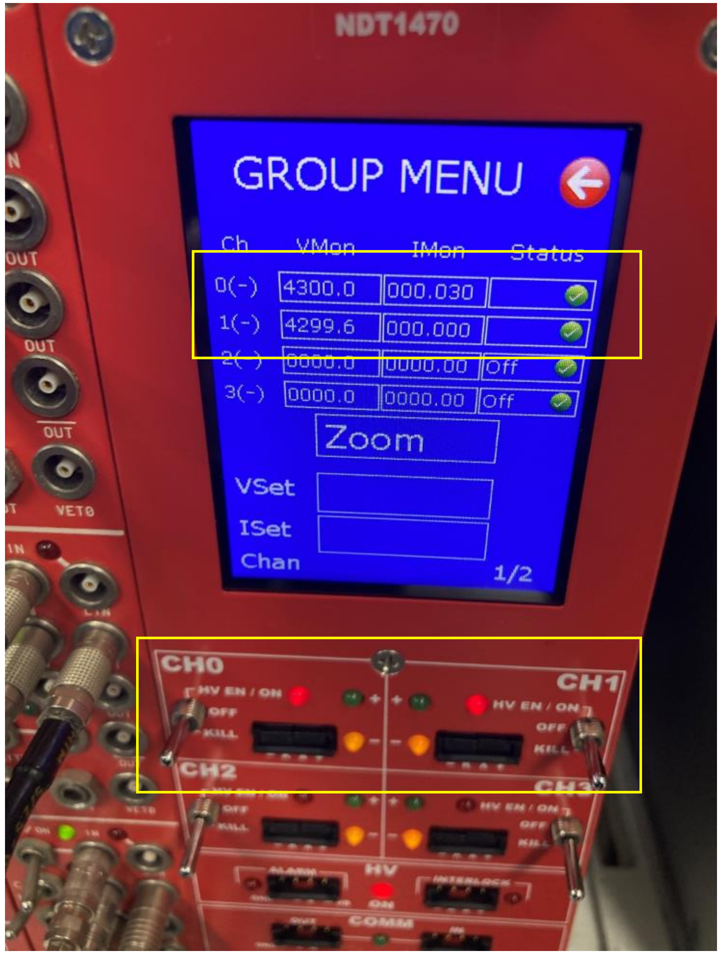
Gas circulation



Connection of HV and signal cable

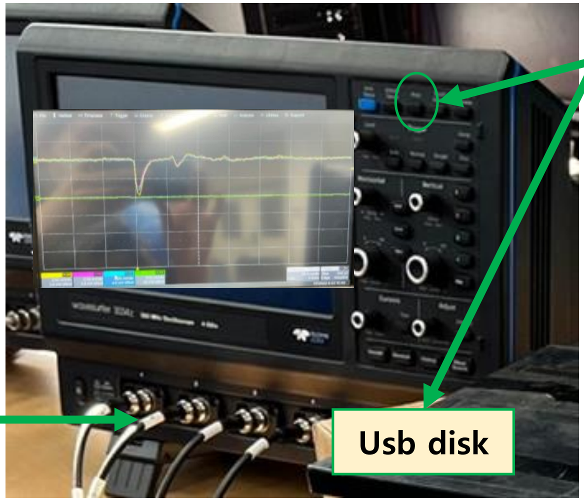


Top → ch0
Bot → ch1



Ch0~4

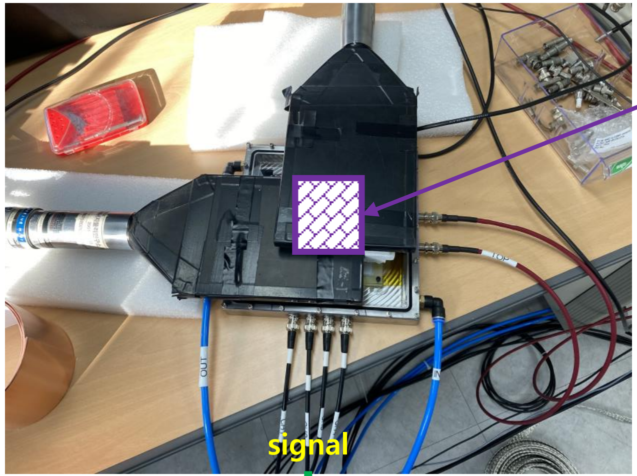
Print signal on the screen on USB disk

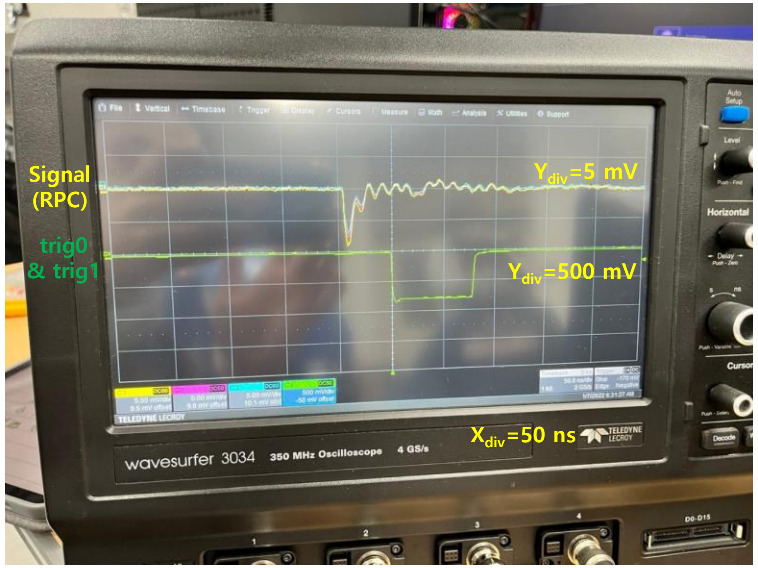


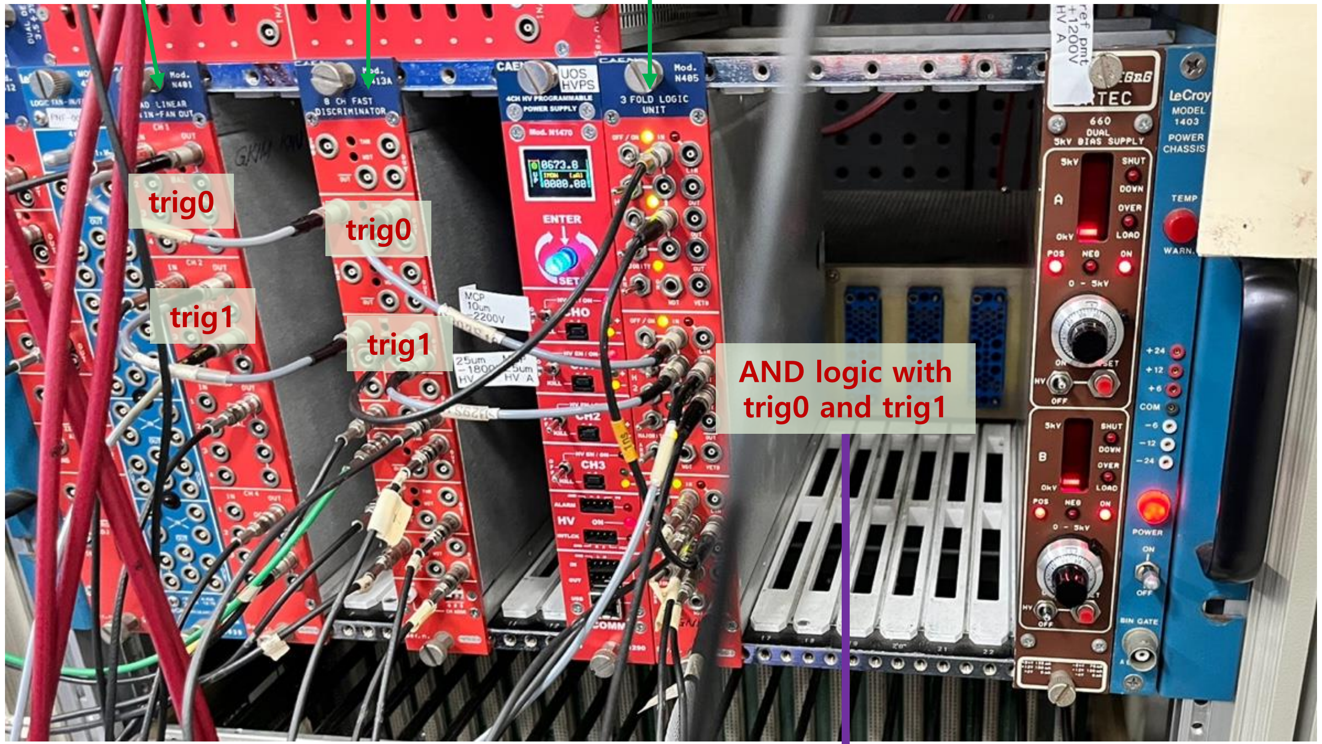
Usb disk

LeCroy wavesurfer 2034
350 MHz (4 GS/s)

Setup of Trigger detector







Amount of signal charge?

Q = it = (V/R) t = ~0.5 (10 mV / 50 ohm) 20 ns = ~2 pC

Number of electron?

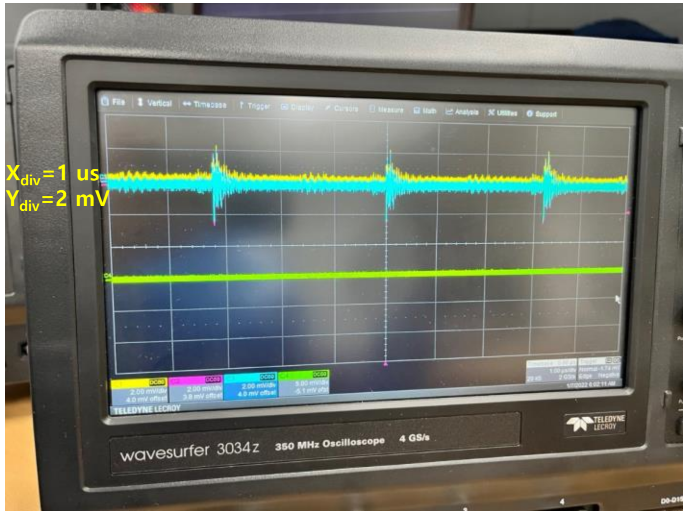
n_e = 2 pC / 1.602 x 10^{-19} C = ~1.3x10^7

[photo] Real test setup of 2RPCs

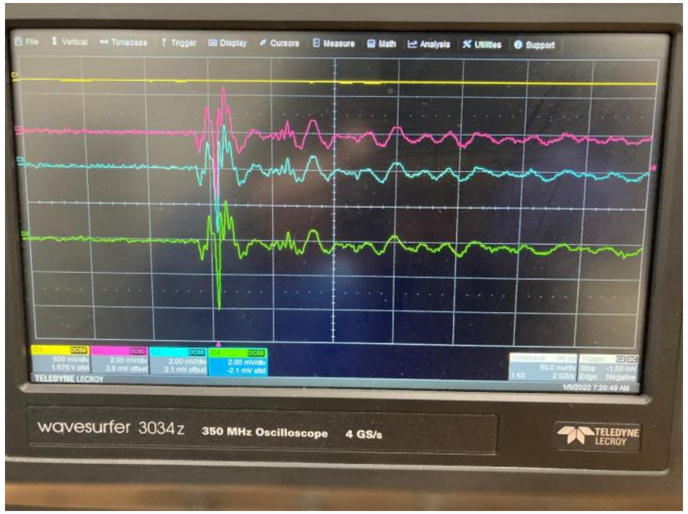
Amount of signal charge?
Q = ~0.5 (1 mV / 50 ohm) 5 ns = ~50 fC

Number of electron?
n_e = 0.05 pC / 1.602 x 10^{-19} C = ~3x10^5

Periodical noise



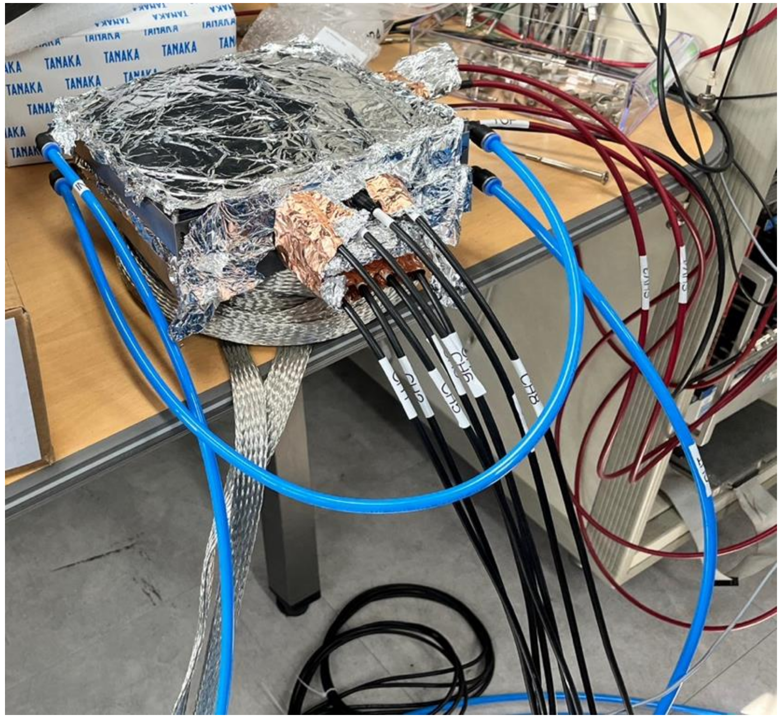
Non-Periodical but frequent noises



<<Removing noise>>

➔ Need bigger GND capacity

➔ Need good connection into electronics



3 coincidence event

Single event of RPC

Daily plan of RPC test in SPDAK 2022

Time	task	parts	Place
09:00~12:00	**저항판 및 spacer 모서리 polishing 가공**	0.7T glass (4ea) 0.5T glass (2ea) 0.5T spacer (4ea)	**216-1호**
	유리판에 전극 및 절연시트 부착 => 전극 10x10 cm^2 재단 => HV (red) & GND (black) cables (4ea) => 절연시트 11x11 cm^2 (6~10ea)	0.7T glass (4ea) 0.2T Mylar sheet (6~10ea)	
	유리판과 spacer 적층 => RPC gap Gap configuration: 0.5/0.5 mm total number of gap: 4 => two gap on both side of readout board pad termination (50 ohm) GND electrode termination (100 kohm)	0.7T glass with Cu electrode (4ea) 0.5T glass (2ea) 0.5T spacer (4ea) readout board with 4 pads (1ea) Thick insulator (2ea) M3x20 plastic screw (4ea)	
	gas vessel에 gap 적층 => Gas leakage test	gas vessel RPC gap M3x10 Stainless screw (?) GND plate	
12:00~13:00	점심		**216-1호**
13:00~15:00	**gas circulation (~60 cc/min = 3.6 L/h)** => total 7.2 L / 0.8L = 9 times circulation **Learn DAQ logic and HV operation**	mixed gas regulator flow meters (100 cc/min)	**지하실험실**
15:00~16:30	**HV ramp up** => 500 V/step till 2000 V (3 min waiting) => 200 V/step till 4000 V (3 min waiting) => 100 V/step till 4800 V (2 min waiting)	waiting time 58 min	
16:30~18:00	**capture the signal with trigger signal** - 3 HV values	check usb disk on oscilloscope	
18:00~19:00	저녁		**216-1호**
19:00~20:00	**finishing test HV ramp down closing the gas valves**		**216-1호**

Glass 및 spacer 재고 현황

부품명	재고 수량 (미사용+사용)	필요 수량 (4 gap)	여분
Glass (0.7T)	16 (10+6)	16	9 new
Glass (0.5T)	18 (16+2)	8	10
Spacer (0.5T)	19 (13+6)	16	3

Glass (0.7 T) 배분 계획

요일	팀	미사용	여분
화	4	4	2
수	3	4	2
목	2	4	2
금	1	4	2

READY TO FABRICATION

Components of waveform

Base line
Pulse height
Pulse width

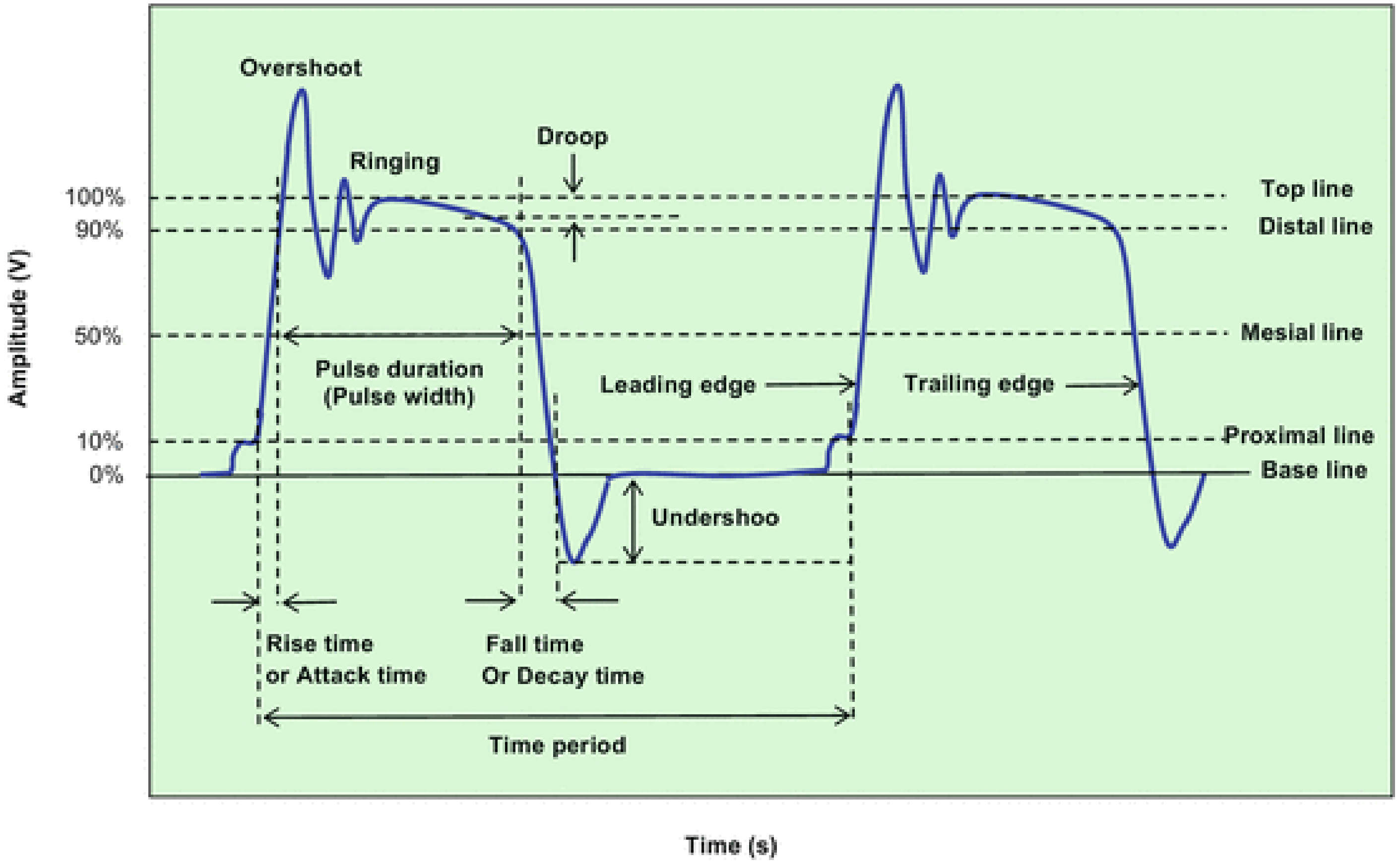
Proximal line: 10% of pulse height
Mesial line: 50% of pulse height
Distal line: 90% of pulse height

Rise time (or attack time) **at leading edge**
Fall time (or decay time) **at trailing edge**
➔ These depend on the polarity of waveform.

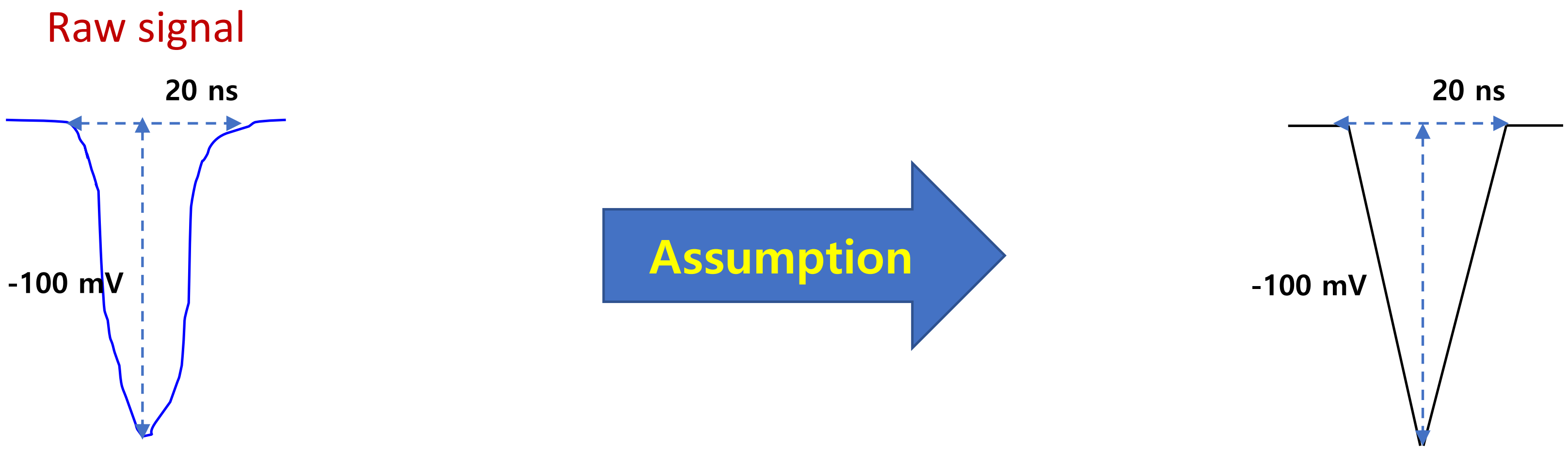
Overshoot
Undershoot
Ringing

Time period

https://link.springer.com/chapter/10.1007/978-3-319-25448-7_7



Charge of raw signal



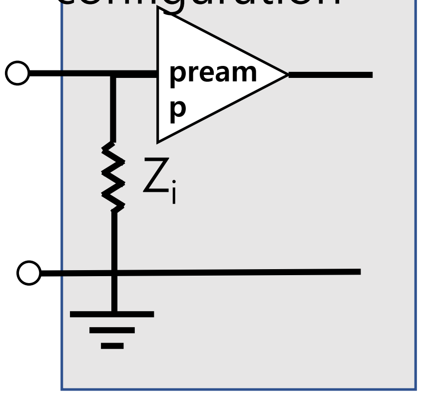
Electric charge of analog signal with assumption:

$$Q(C) = \frac{V(V) \cdot t(s)}{2 \cdot R(\Omega)} = \frac{-0.1\,V \cdot 20\,ns}{2 \cdot 50\Omega} = -20\,pC$$

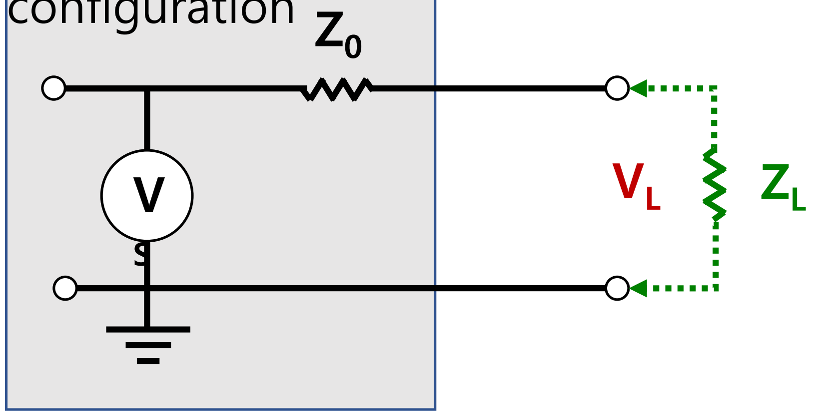
Device impedances

A basic concept in the processing of pulses from radiation detectors is the impedance of the devices that comprise the signal-processing chain.

Input configuration



output configuration



Voltage (V_L) appearing across a loading (Z_L) by voltage-divider relation

$$V_L = V_S \frac{Z_L}{Z_0 + Z_L}$$

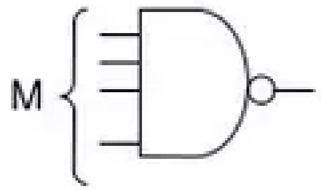
For the open-circuit or unloaded ($Z_L = \infty$), voltage is $V_L = V_S$. ➔ not for the real experiment

To preserve maximum signal level, one normally wants V_L to be as large a fraction of V_S as possible.
For $Z_L \gg Z_0$ then $V_L \cong V_S$ ➔ Fan-In & Fan-Out, Discriminator, ADC, etc

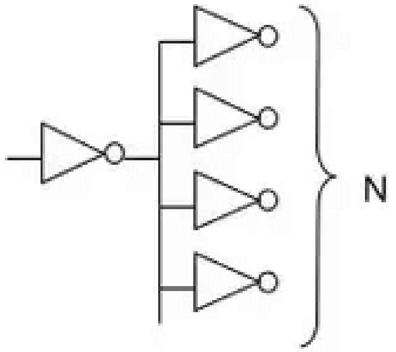
For $Z_L = Z_0$ then $V_L = V_S/2$ ➔ Divider or Splitter

Fan-In and Fan-Out (FIFO)

Fan-in: maximum number of input signals feeding into the input of a logic system

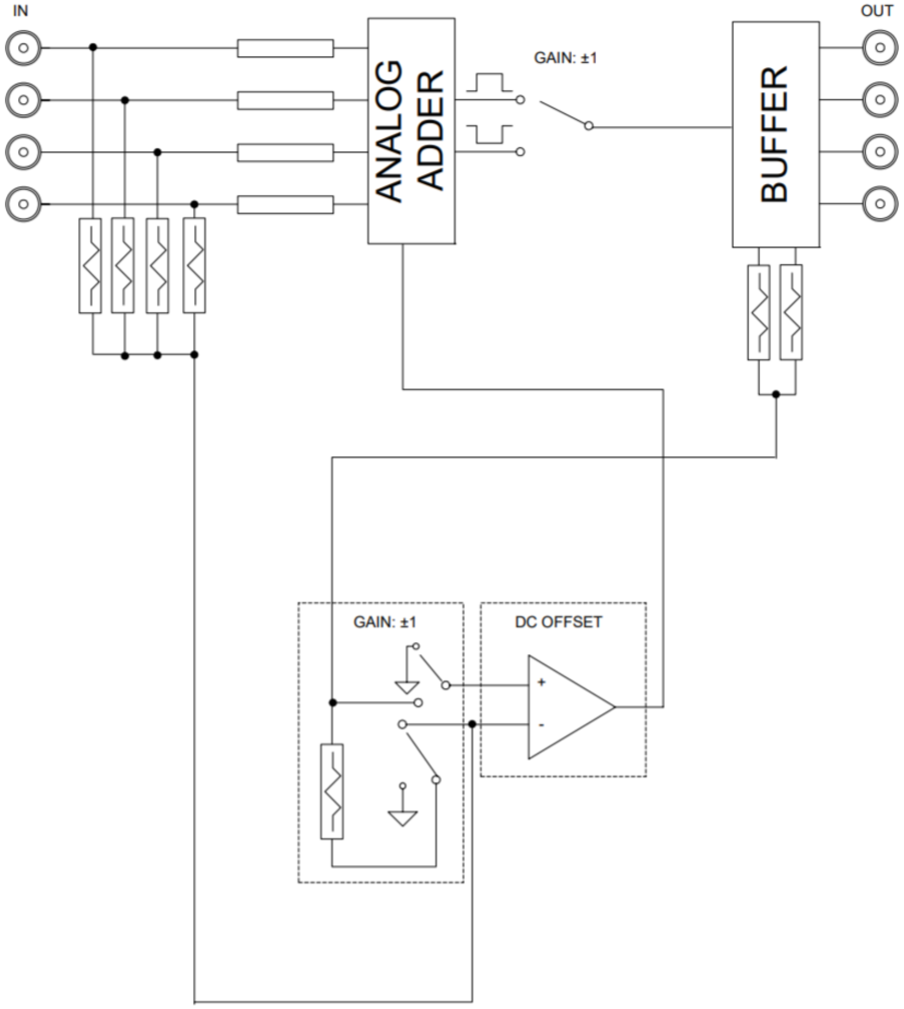


Fan-out: maximum number of output signals from the output of a logic system

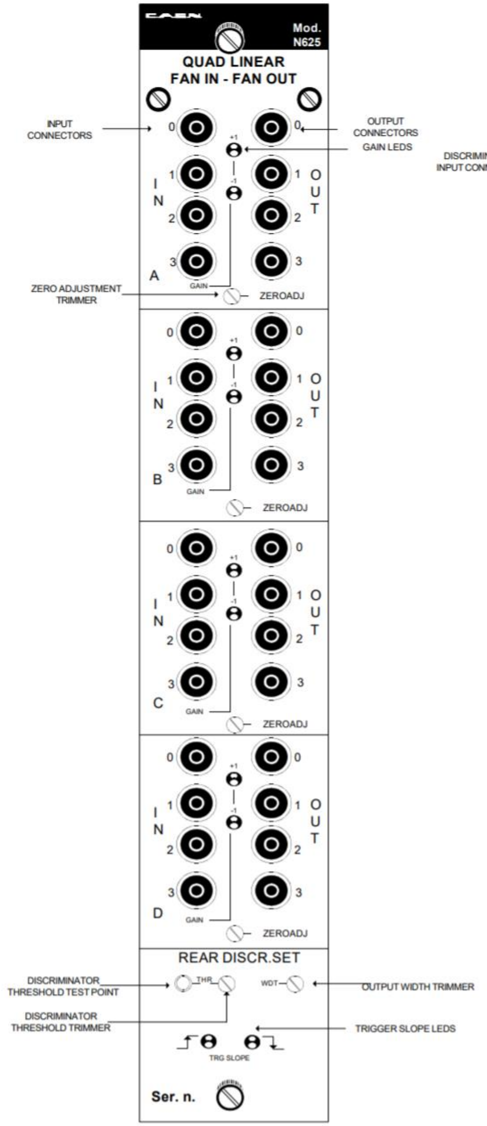


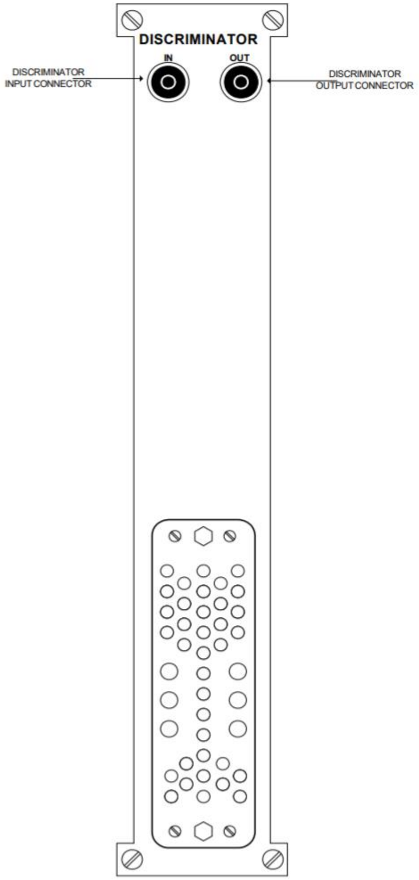
Fan-In and Fan-Out (FIFO)

https://www.caen.it



CAEN N625 Quad Linear Fan In / Fan Out



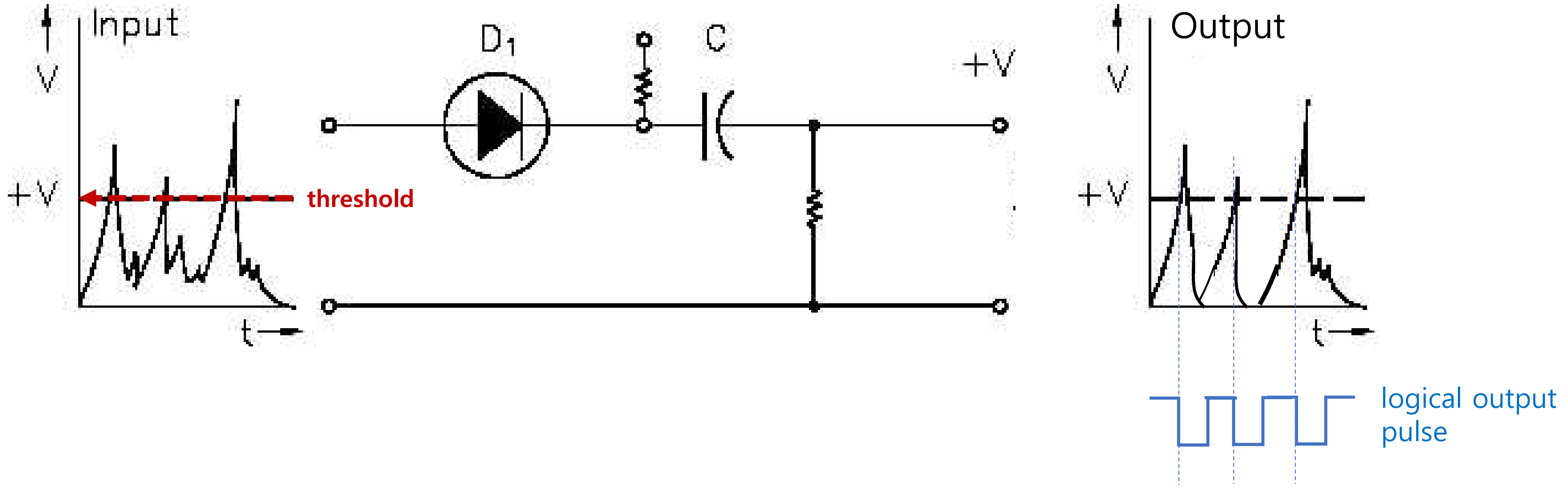


Discriminator (DISC)

http://nuclearpowertraining.tpub.com/h1013v2/css/Discriminator-Circuit-83.htm

Role: generating the logical output pulse when the input pulse exceeds the discriminator preset level

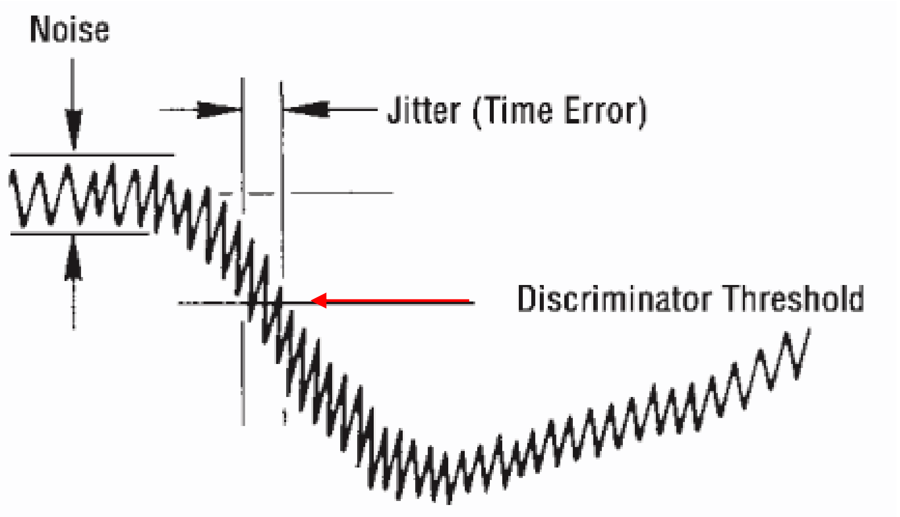
➔ If input voltages **exceeds the threshold value +V** then diode D_1 conducts and **DISC generates the logical output pulses**.



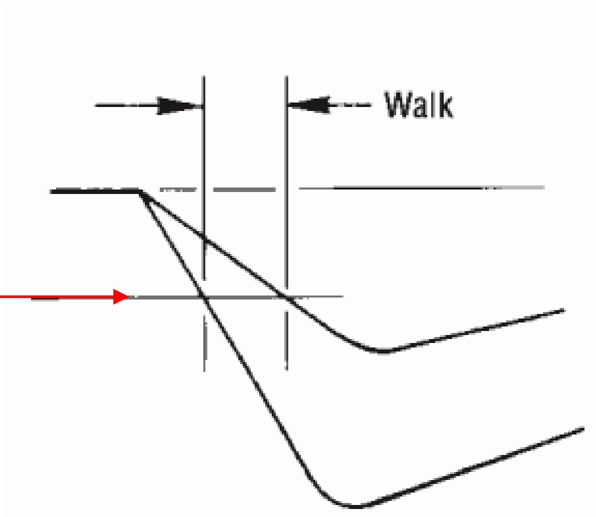
Timing jitter and walk

http://www.peo-radiation-technology.com/wp-content/uploads/2015/09/ort_15_fast-timing-discriminators_datasheet_peo.pdf

Timing jitter in a pulse



Timing walk among pulses



The contribution of noise to the (Timing) Jitter

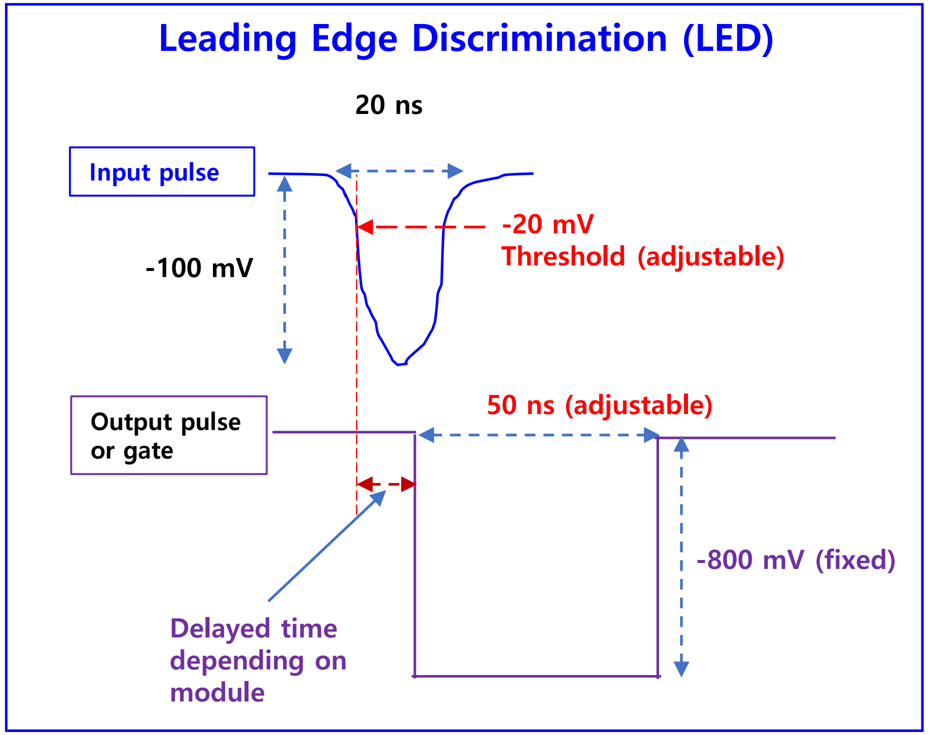
$$\textbf{Timing Jitter} = e_{noise}/(dV/dt)$$

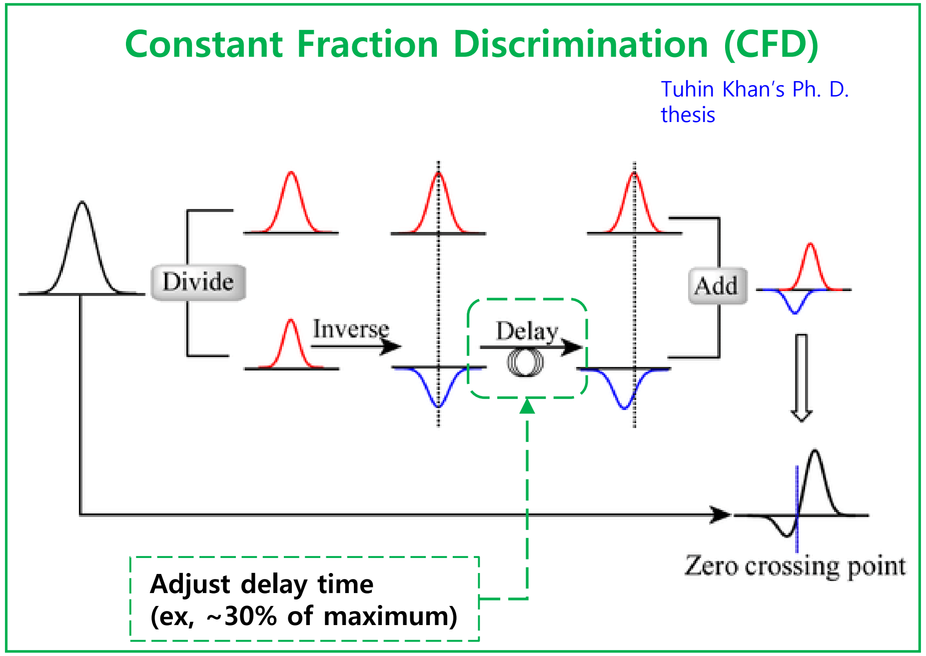
e_{noise}: voltage amplitude of the noise superimposed on the analog pulse

dV/dt: slope of the signal when its leading edge crosses the discriminator threshold

"(Timing) Walk" is the **systematic dependence** of the time marker **on the amplitude of the input pulse.**

Discriminator (DISC)





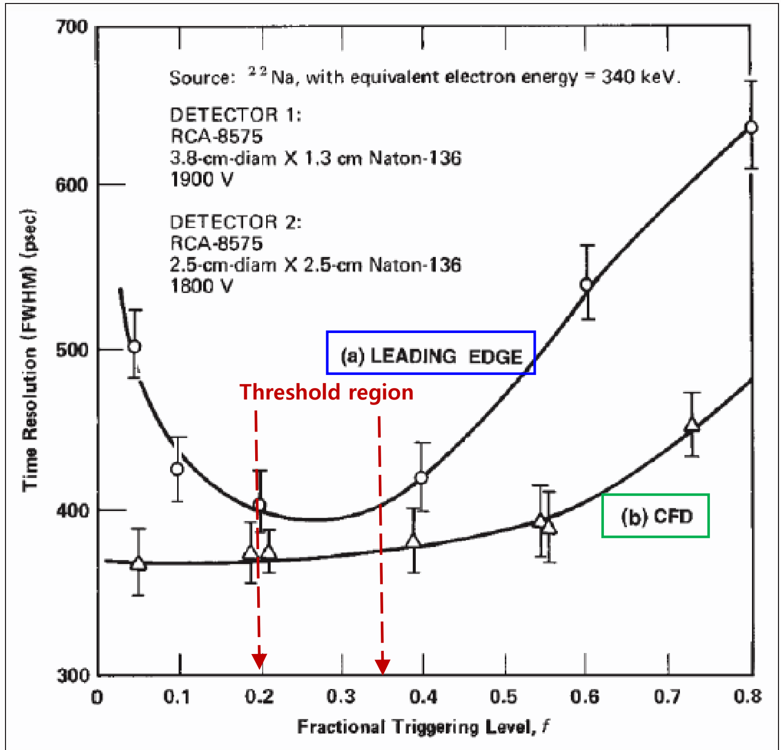


Fig. 2. A Comparison of Leading-Edge Timing with Constant-Fraction Timing for a Narrow Pulse-Height Range. The source was ^{22}Na, with the selected equivalent electron energy in the scintillator = 340 keV. The time resolution (FWHM) is Δ t.

http://www.peo-radiation-technology.com/wp-content/uploads/2015/09/ort_15_fast-timing-discriminators_datasheet_peo.pdf

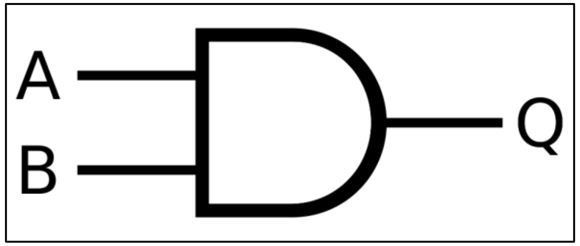
Time resolution: $\sigma_{CFD} < \sigma_{LED}$

Logic Unit

https://www.wekipedia.com

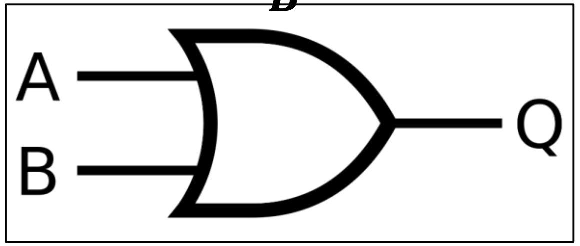
Role: generating the gating pulse when the preset of logical algorism against with inputs is true

AND logic: $\boldsymbol{A \cdot B}$ **or** $\boldsymbol{A \wedge B}$



INPUT		OUTPUT
A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1

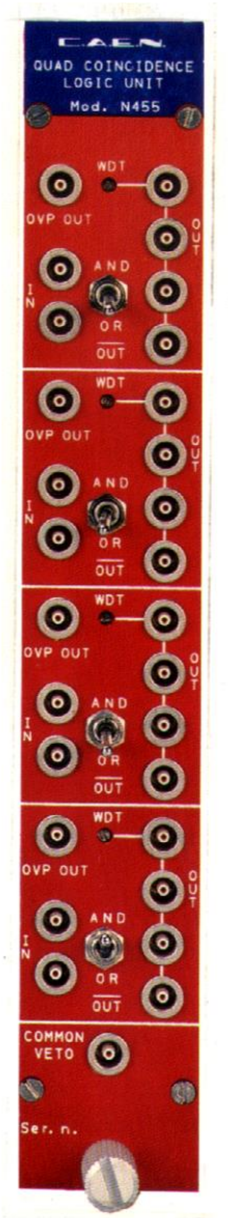
OR logic: $\boldsymbol{A + B}$ **or** $\boldsymbol{A \vee B}$

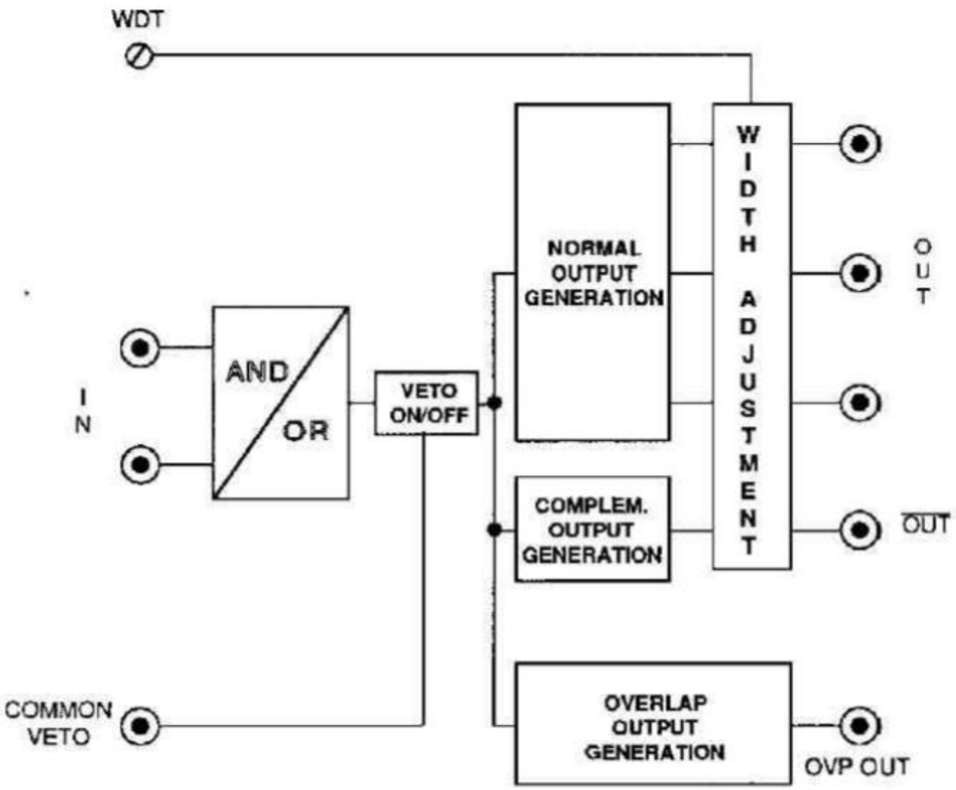


INPUT		OUTPUT
A	B	Q
0	0	0
0	1	1
1	0	1
1	1	1

Logic Unit

https://www.caen.it



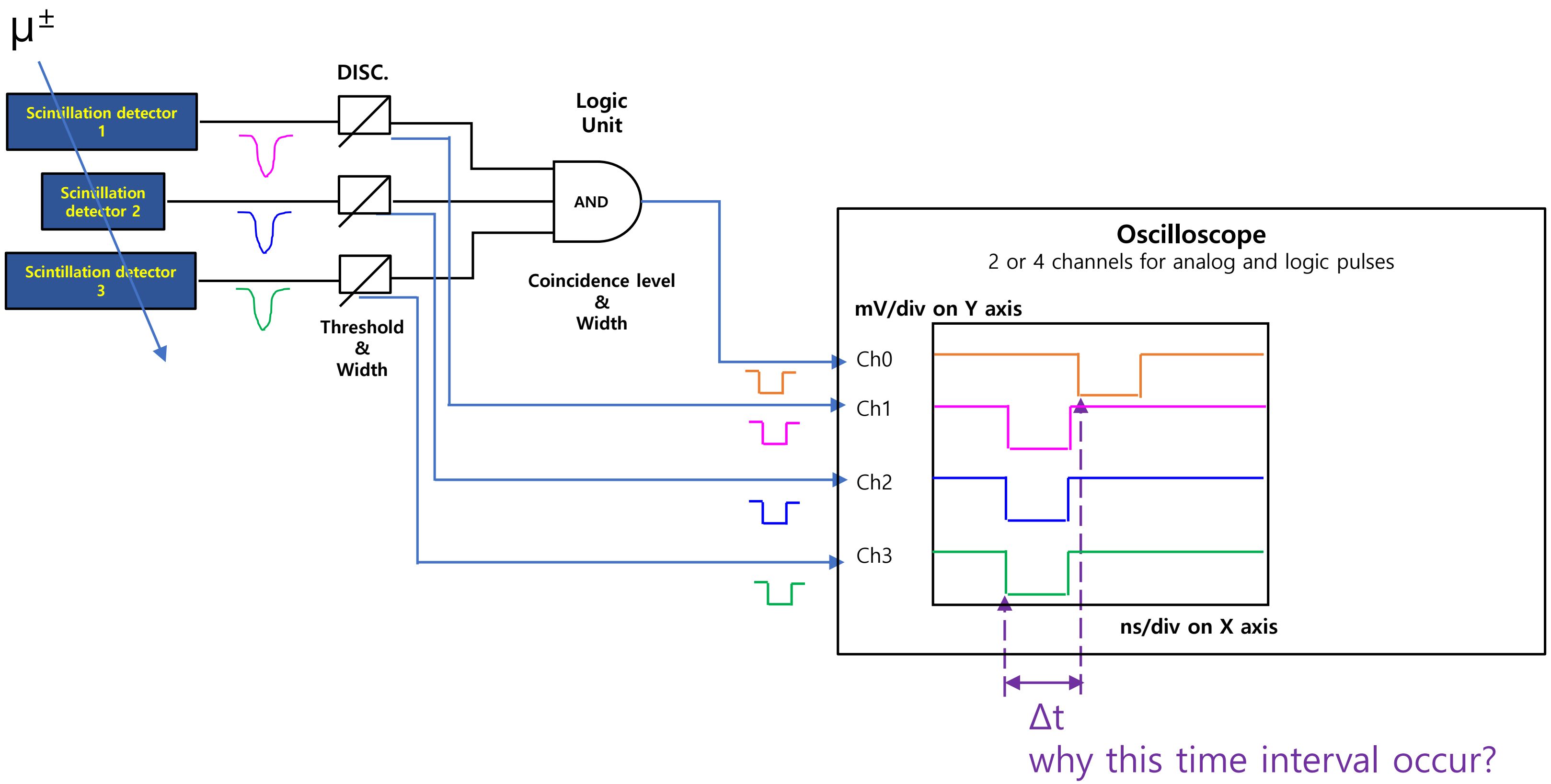


IMPORTANT NOTE:
Unused Outputs require a 50 Ω termination

CAEN N455 Quad Coincidence Logic Unit

INTRODUCTION: Is it possible to watch the signal from detectors?

Scintillation counter/detector:
Scintillator + **P**hoto**M**ultiplier **T**ube (PMT)



Question> What is difference between scintillation counter and detector?

counter: just counting how many particles passed through it

detector: measure time and charge to get position, energy, dE/dx, and so on