KNU 검출기학교 2022

Fast electronics and DAQ

김상열

노티스

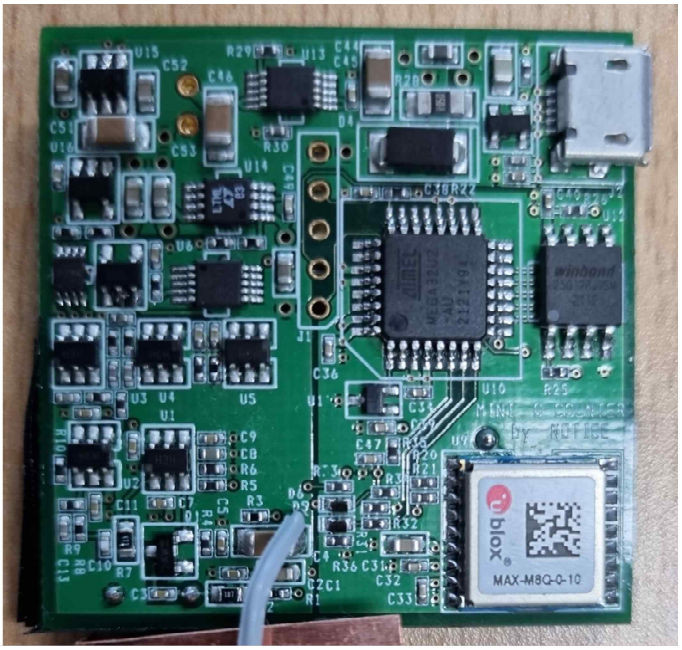
Why Electronics?

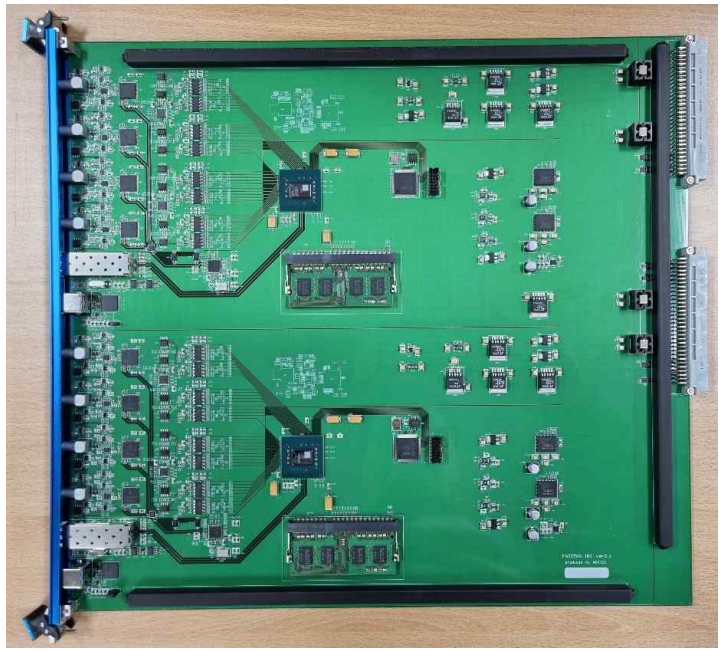
Detector + Electronics + Analysis = Experiment

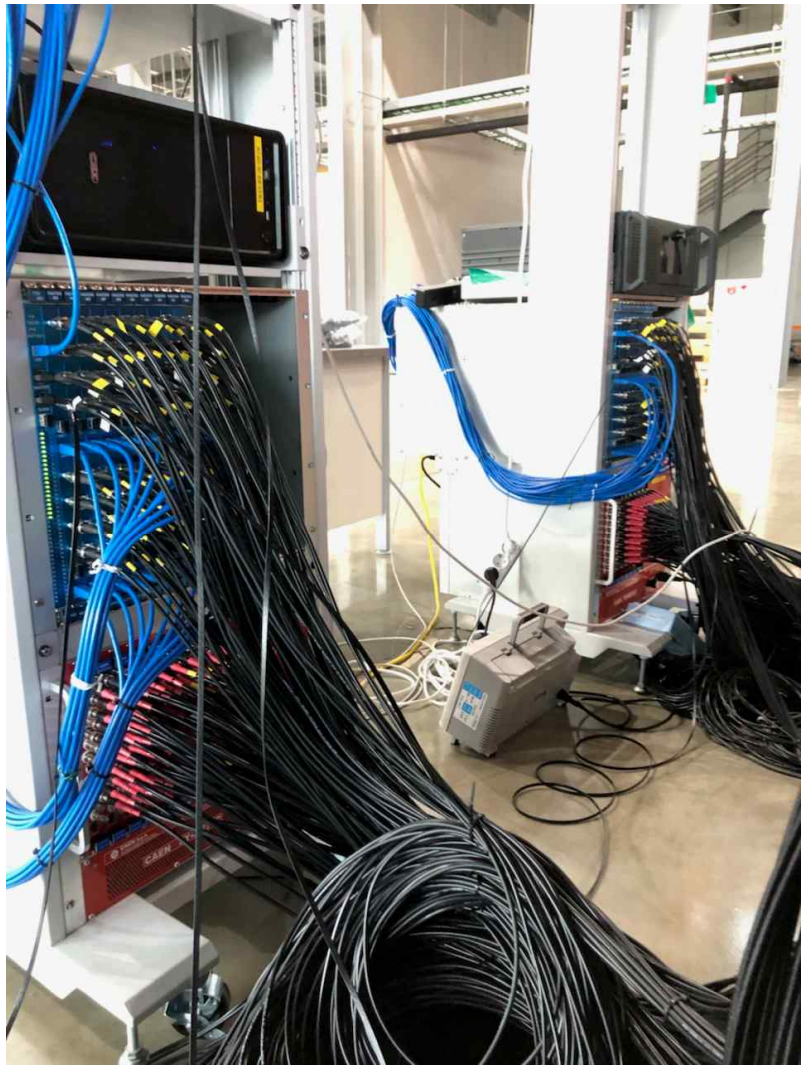
Detector + Electronics + X = Development

X + Electronics + Analysis = Not Bad?

Detector + X + Analysis = ????


MAX-M8Q-0-10





We will see :

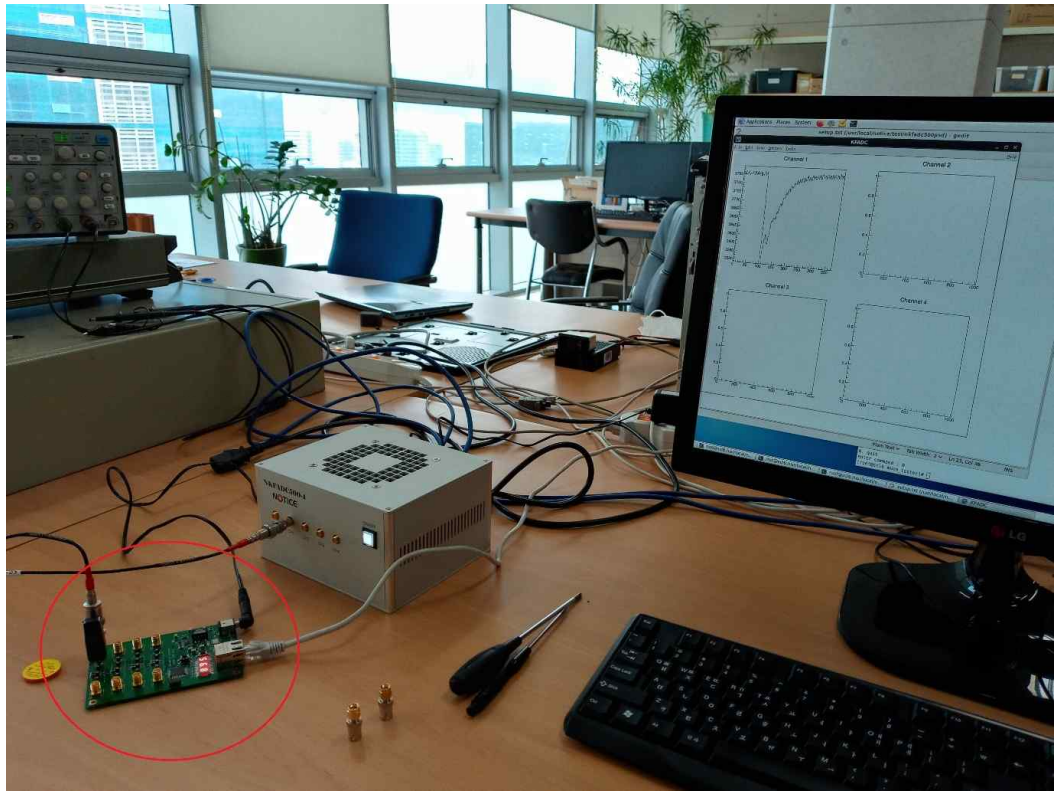
1. What electronics are used?

2. How they work?

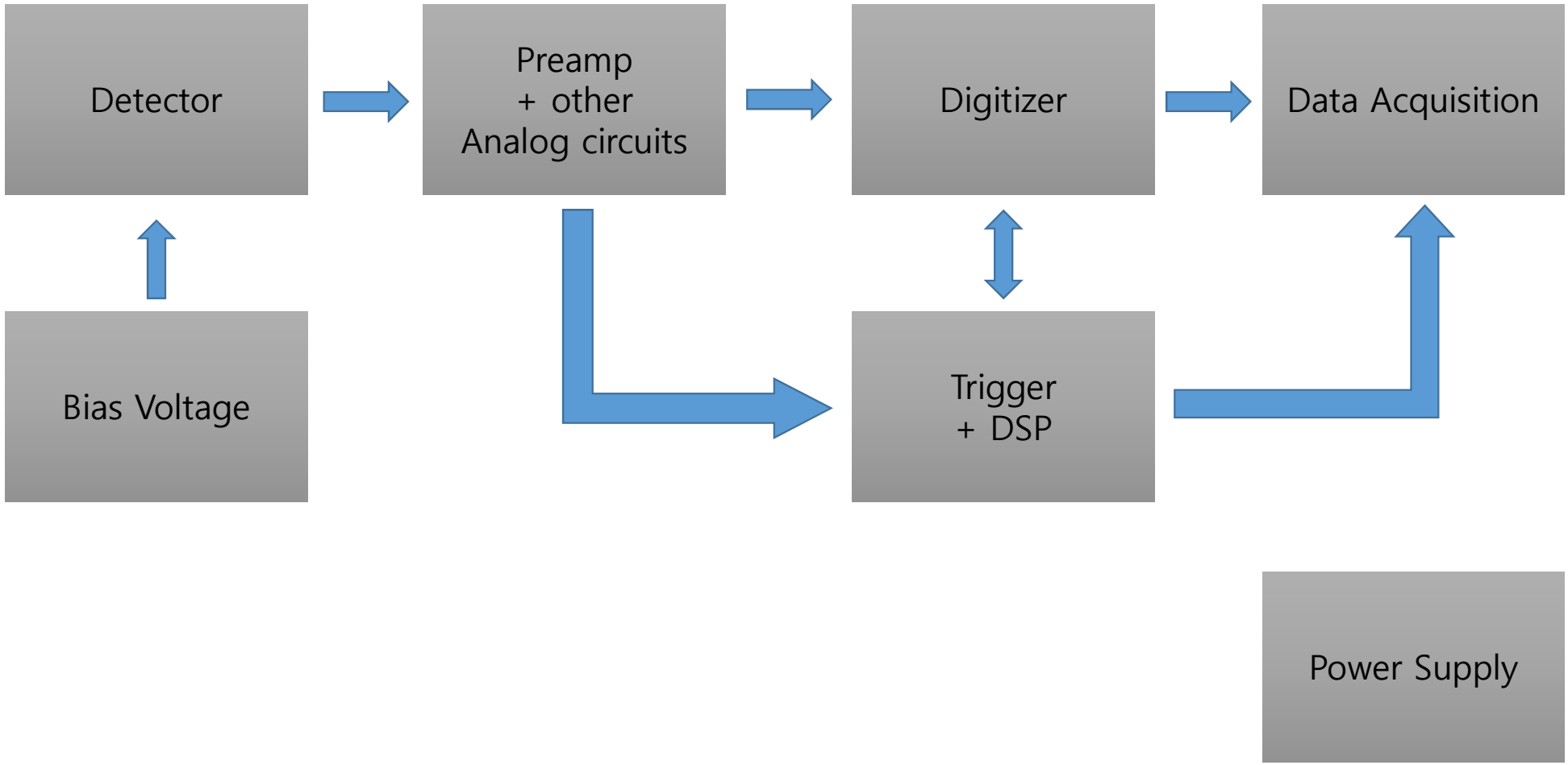
3. How to make them?

~~4. Where to sell?~~

Goal :



Electronics for High energy or Nuclear physics experiment



Frequently used example

50 ohm input impedance

Oscilloscope level trigger

Signal from some detectors

PMT, SiPM… : gain ~ 10^6
-> ~ 10^10 electrons/MeV
= ~ nC/MeV

Wire chamber, GEM… : gain ~ 10^2~3
-> ~ 10^6~7 electrons/MeV
= ~ pC/MeV

Photodiode, Ion chamber… : gain ~ 1
-> ~ 10^3~5 electrons/MeV
= ~ fC/MeV

How to measure signal

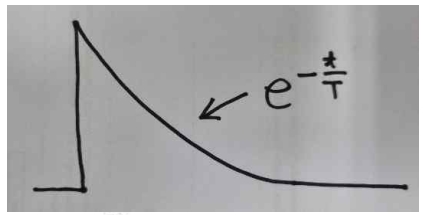
Typical detector's capacitance
= 10 ~ 1000 pF
and V = Q/C

~ nC/100 pF/MeV = ~ V/MeV (OK)

~ pC/100 pF/MeV = ~ mV/MeV (?)

~ fC/100 pF/MeV = ~ uV/MeV (X)

What we measure actually? Charge? Current?



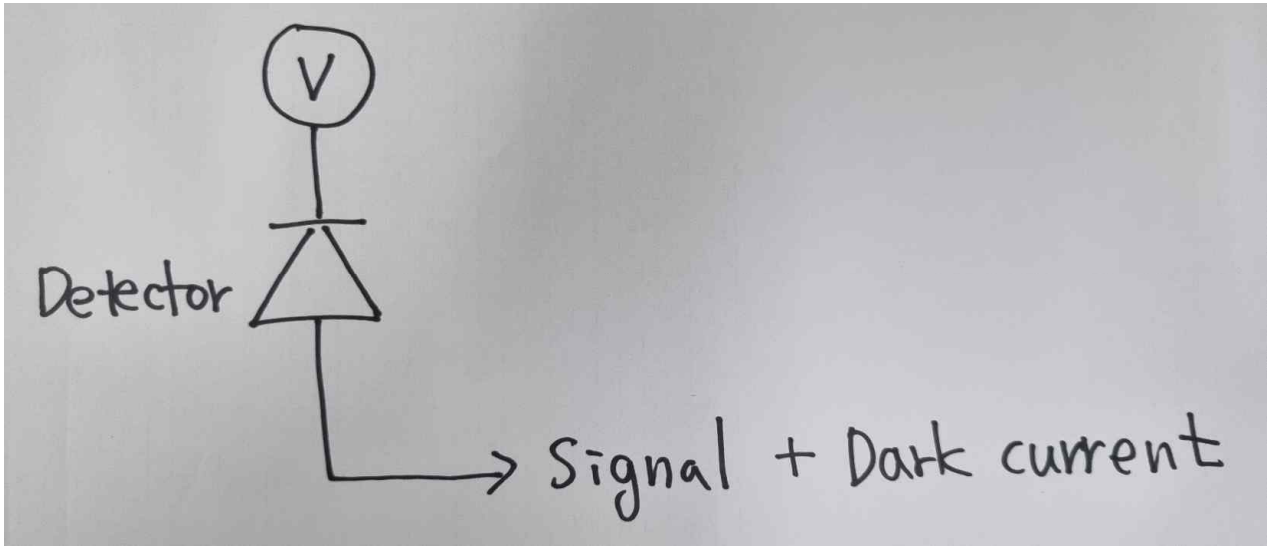
When Idet(detector current) is very fast,

Isig = Qdet x exp(-t/T) where T = Cd x Rm = 100 pF x 10 Mohm

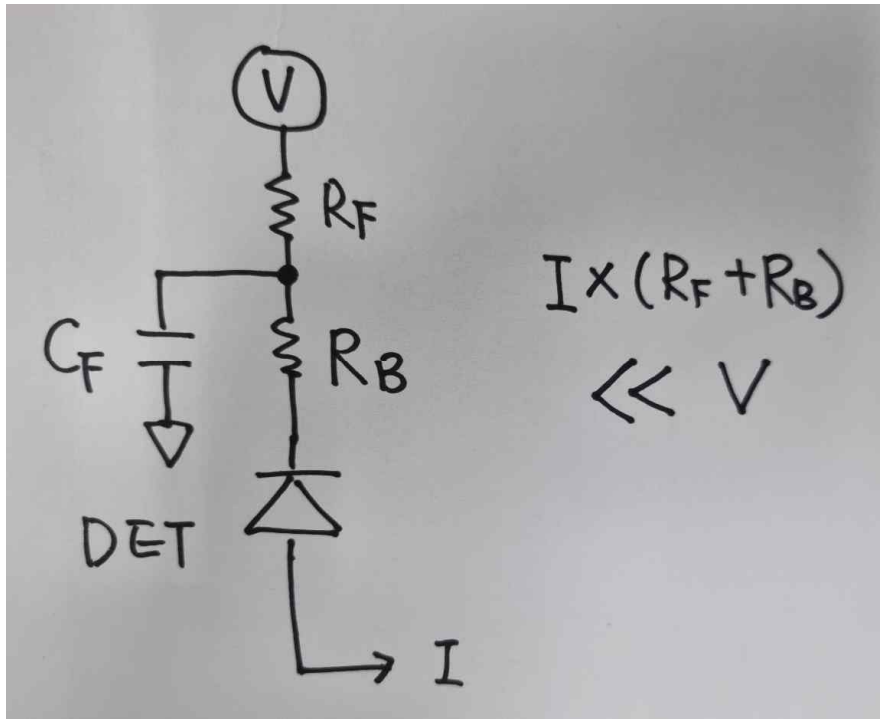
= ~ ms -> very long!

Detector signal :

Where it comes from? = Bias Voltage Source (few ~ 10,000 V)

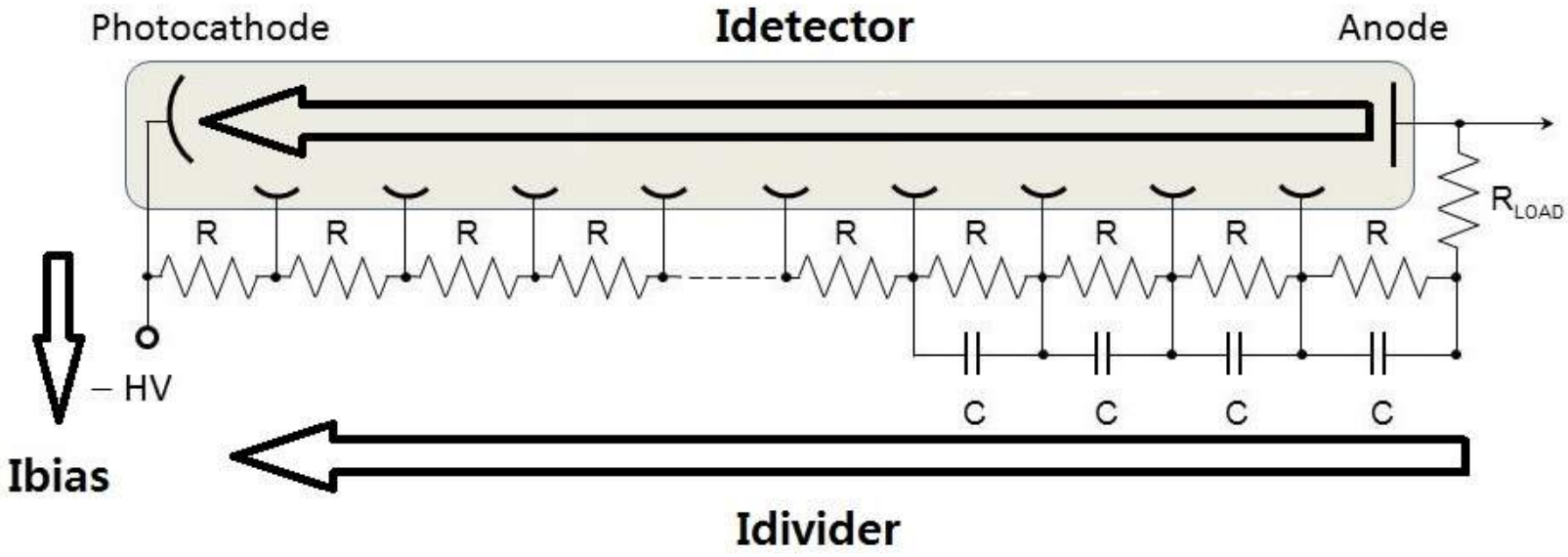


Ibias(max) > Isig + Idark
Isig = Signal x Count rate



Bias Filter

PMT example



Ibias = Idetector + Idivider

$$\text{Qdetector} = \int \text{Idetector}\, dt$$

Usually Idivider >> Idetector (100 times or greater)

Bias voltage supplier should supply

If count rate = ~ 100 kcps (when no Dark current)

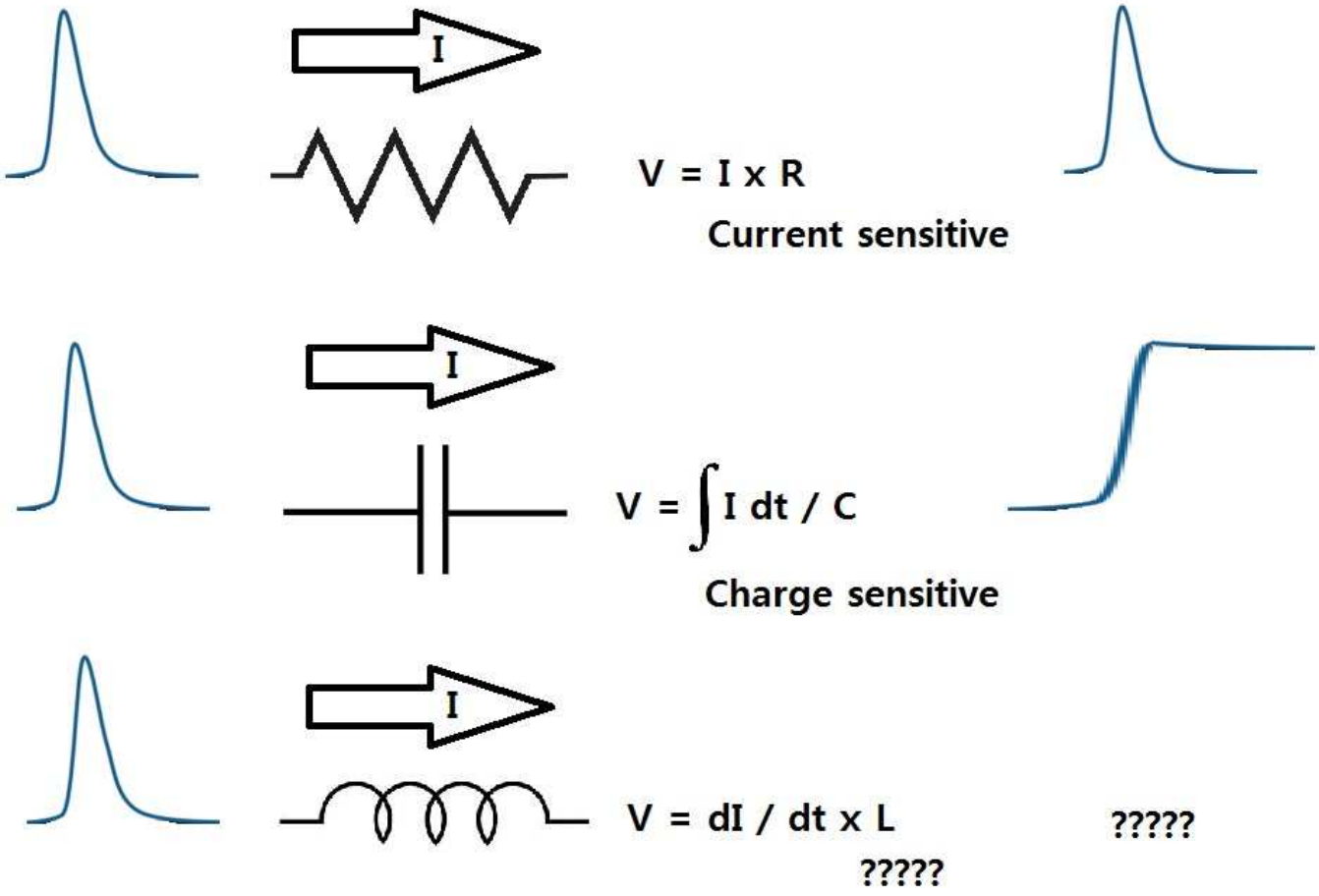
PMT : nC x 100 kcps x (10 ~ 100 : Divider)
= 10 uA -> 1 mA @ a few kV -> W

SiPM : nC x 100 kcps
= 10 uA @ 20 ~ 60 V -> mW

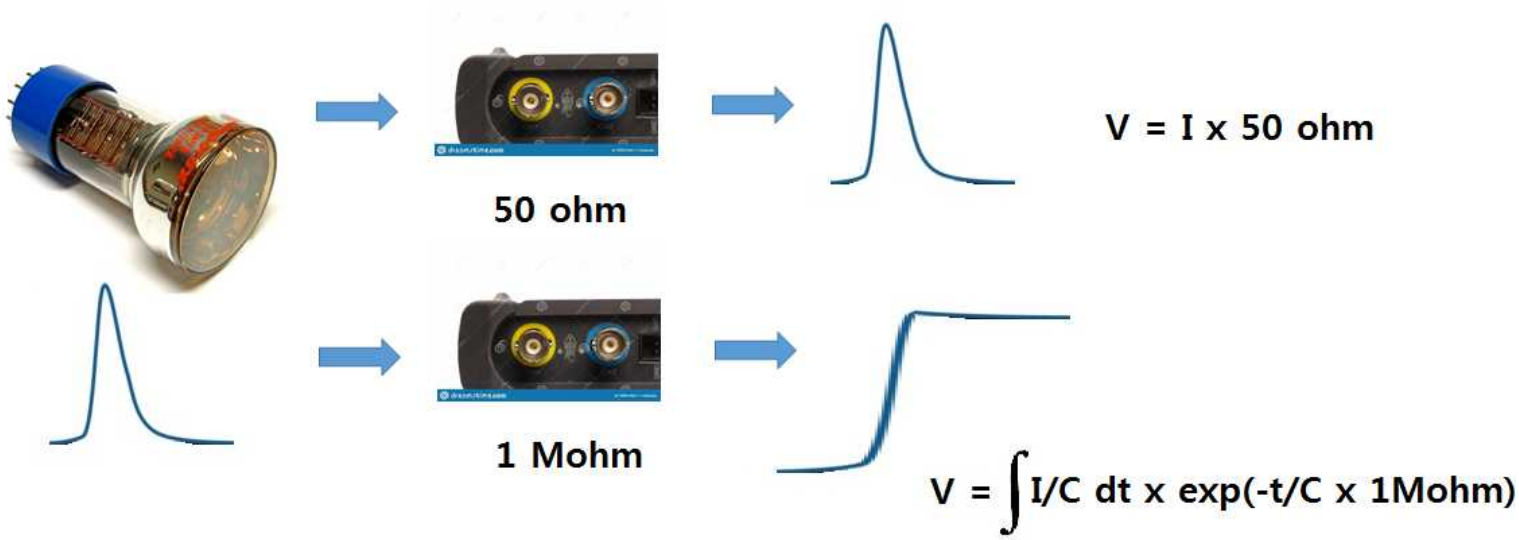
Wire chamber, GEM… : pC x 100 kcps
= 0.1 uA @ kV -> mW

Photodiode, Ion chamber… : fC x 100 kcps
= ~1 nA @ a few ~ kV -> uW

First thing to do :
Preamplifier converts Idet to Voltage signal.

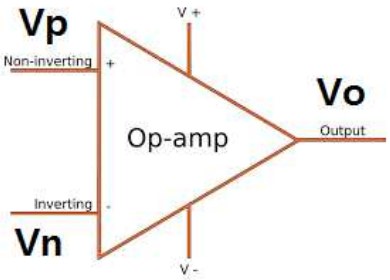


Take a look at PMT oscilloscope shot again



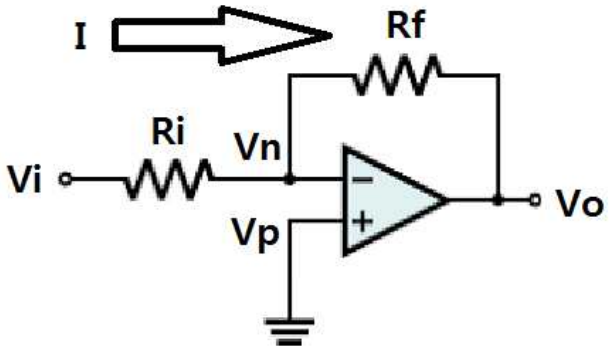
What happens if detector response is very short?

OpAmp basics



$$V_o = A \times (V_p - V_n)$$

where A is very large



$$V_p = 0$$

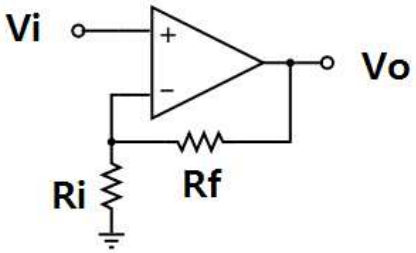
$$V_n = V_i - R_i \times I$$

$$V_o = V_n - R_f \times I$$

$$= A \times (V_p - V_n)$$

$$V_0 = -V_i \times \frac{R_f}{R_i} \times \frac{1}{1 + [(1 + R_f/R_i) / A]}$$

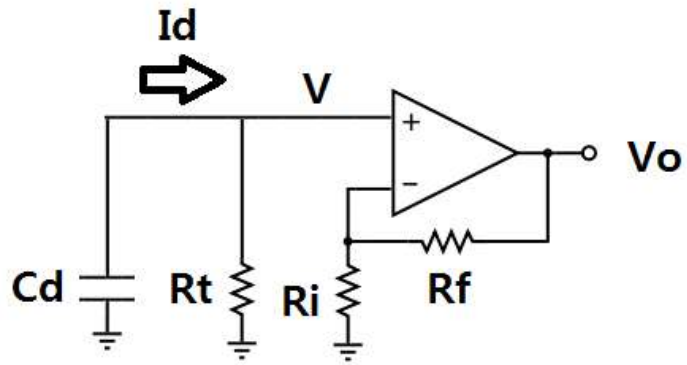
$$= -V_i \times R_f/R_i$$



Similary,

$$V_o = V_i \times (1 + R_f/R_i)$$

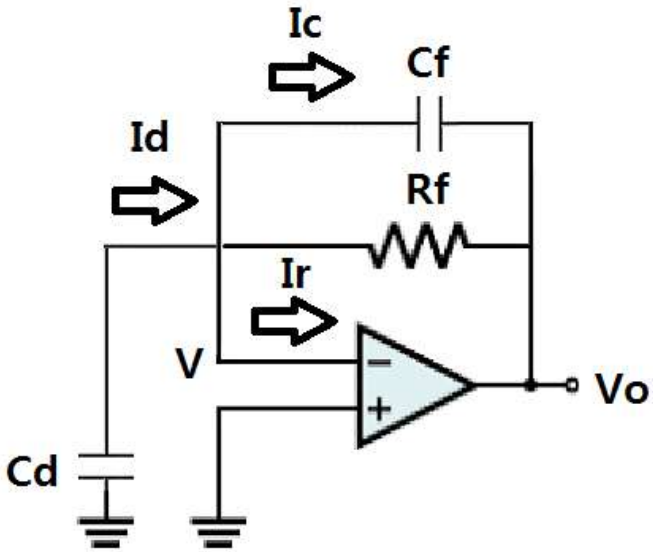
Current Sensitive Preamp



$V = Q_d / C_d = I_d \times R_t = -dQ_d/dt \times R_t$

$Q_d = Q \times \exp(-t/R_t \times C_d)$

$V_o = (1 + R_f/R_i) \times Q/C_d \times \exp(-t/R_t \times C_d)$

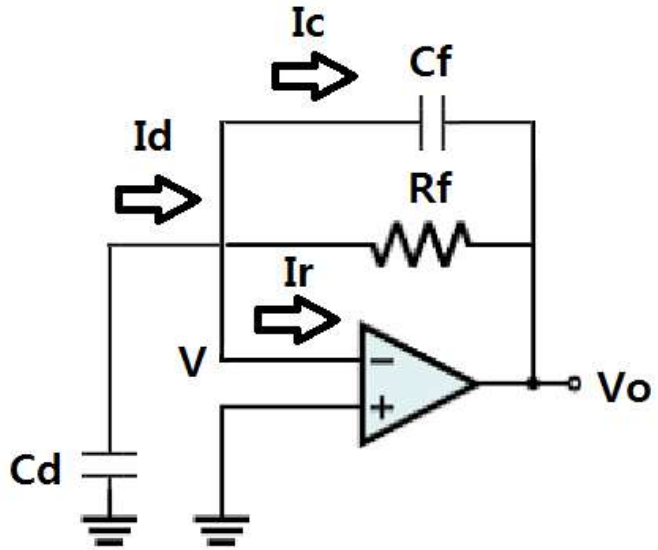


If $I_r \gg I_c$, $I_r = I_d$

$V - V_o = -V_o = I_r \times R_f$

$V_o = -I_d \times R_f$

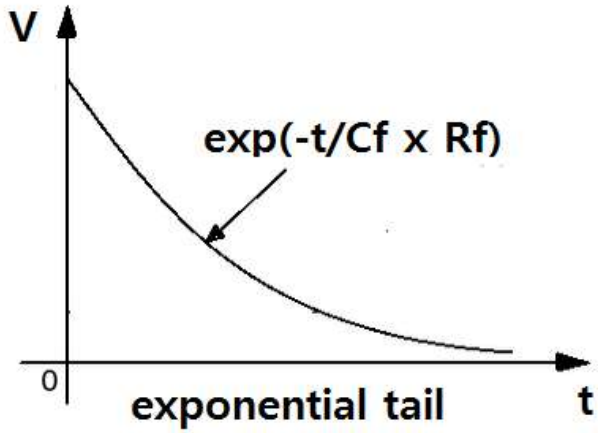
Charge Sensitive Preamp



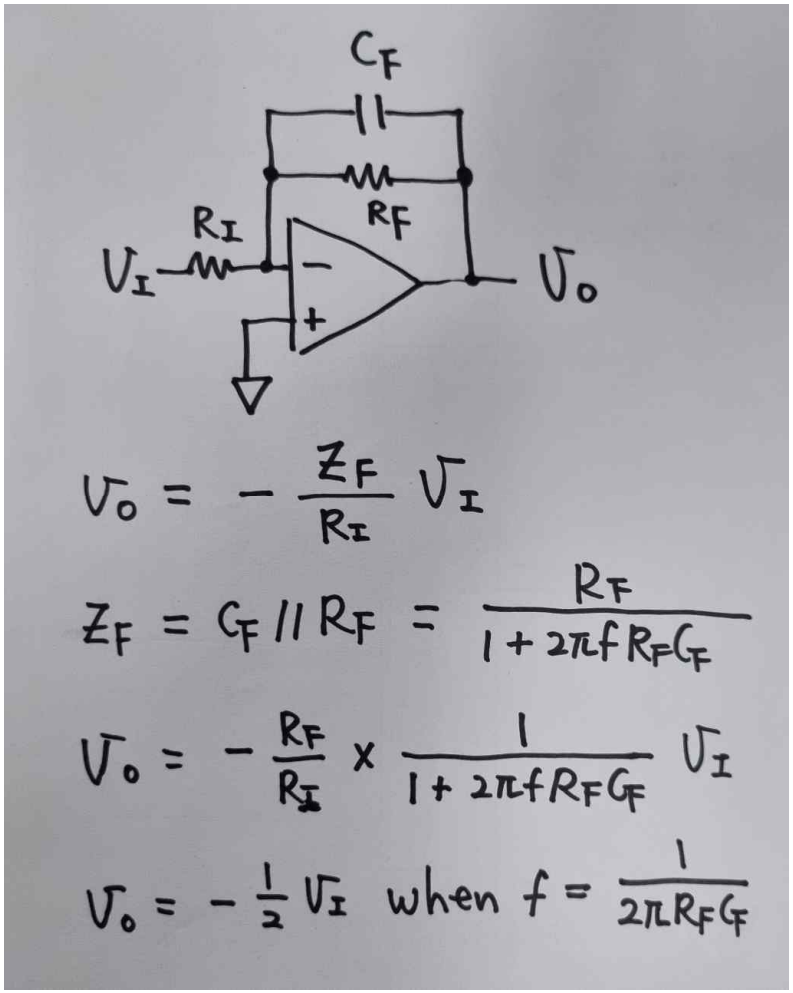
If Ic >> Ir, Ic = Id

$$V - V0 = -V = \int Ir\ dt \times 1/Cf$$

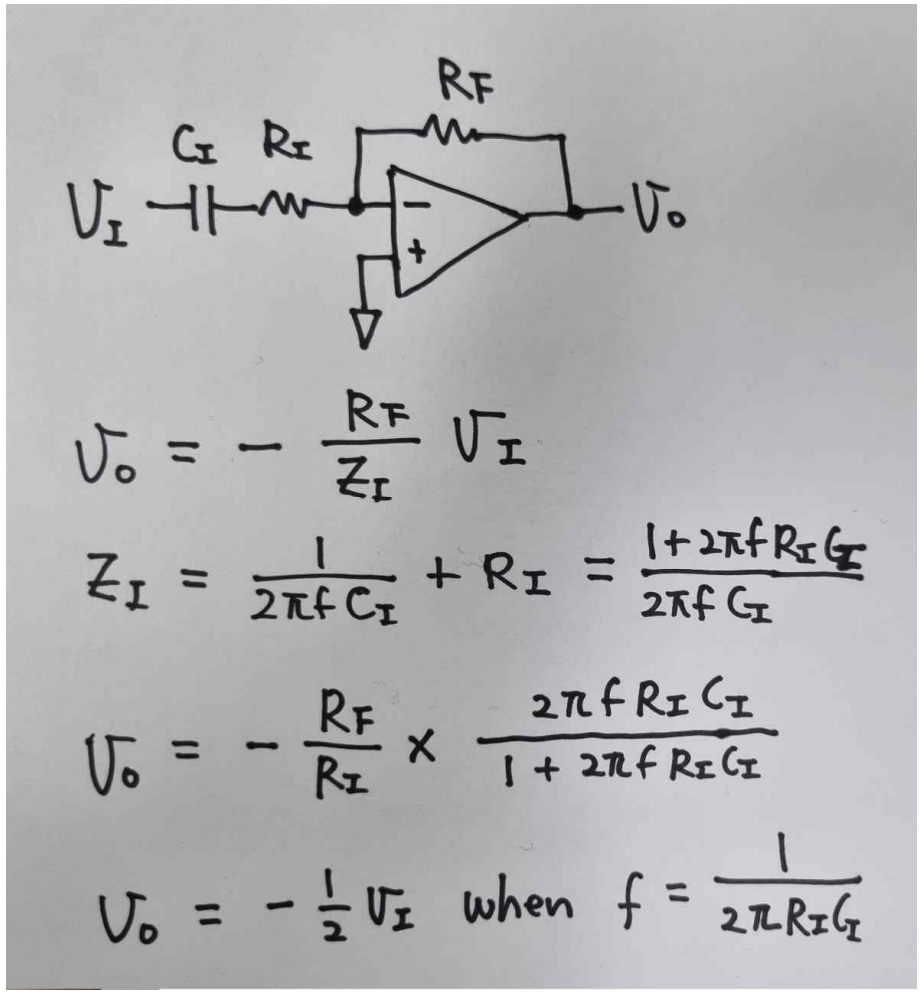
$$Vo = -1/Cf \times \int Id\ dt = -Qd/Cf$$



Filter : Modify preamplifier pulse to better shape for later stage

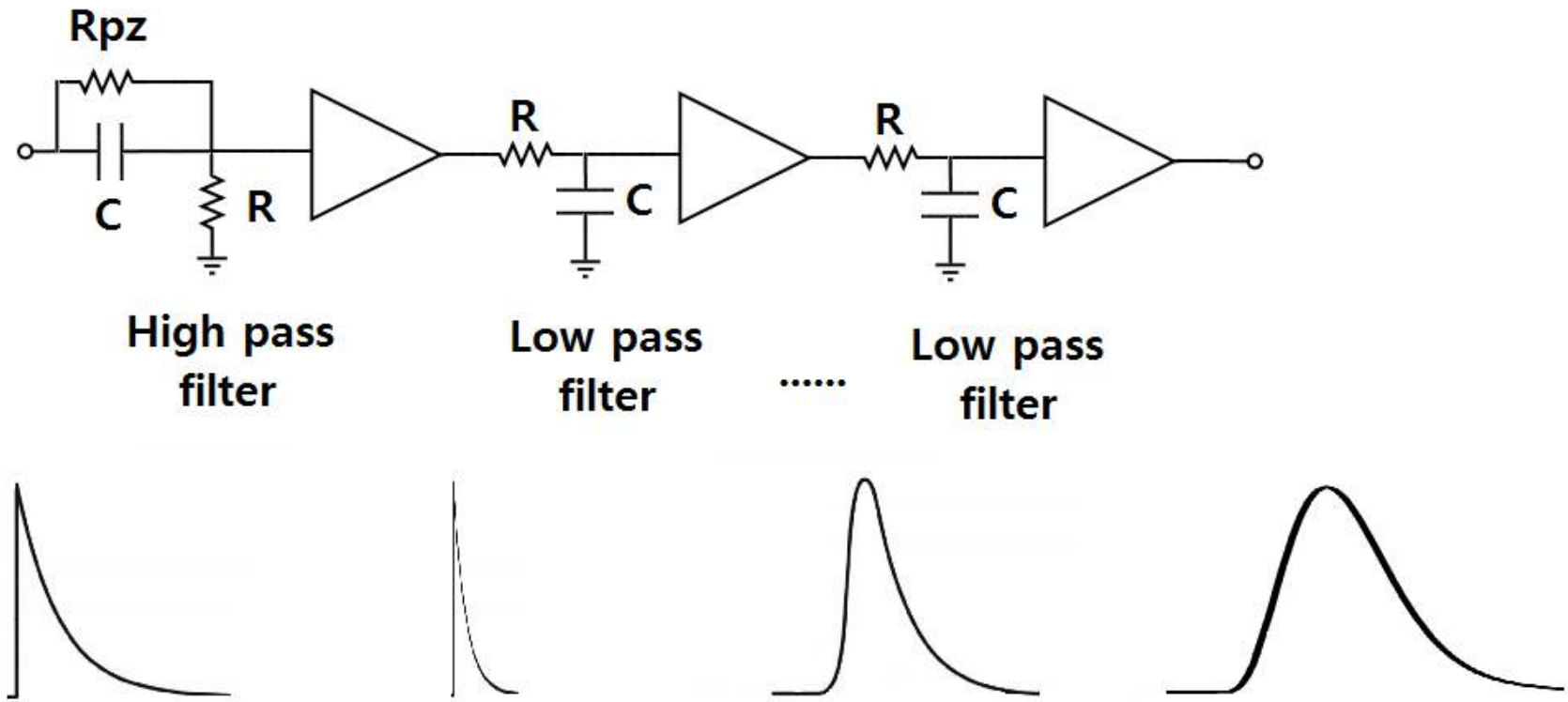


Low Pass Filter

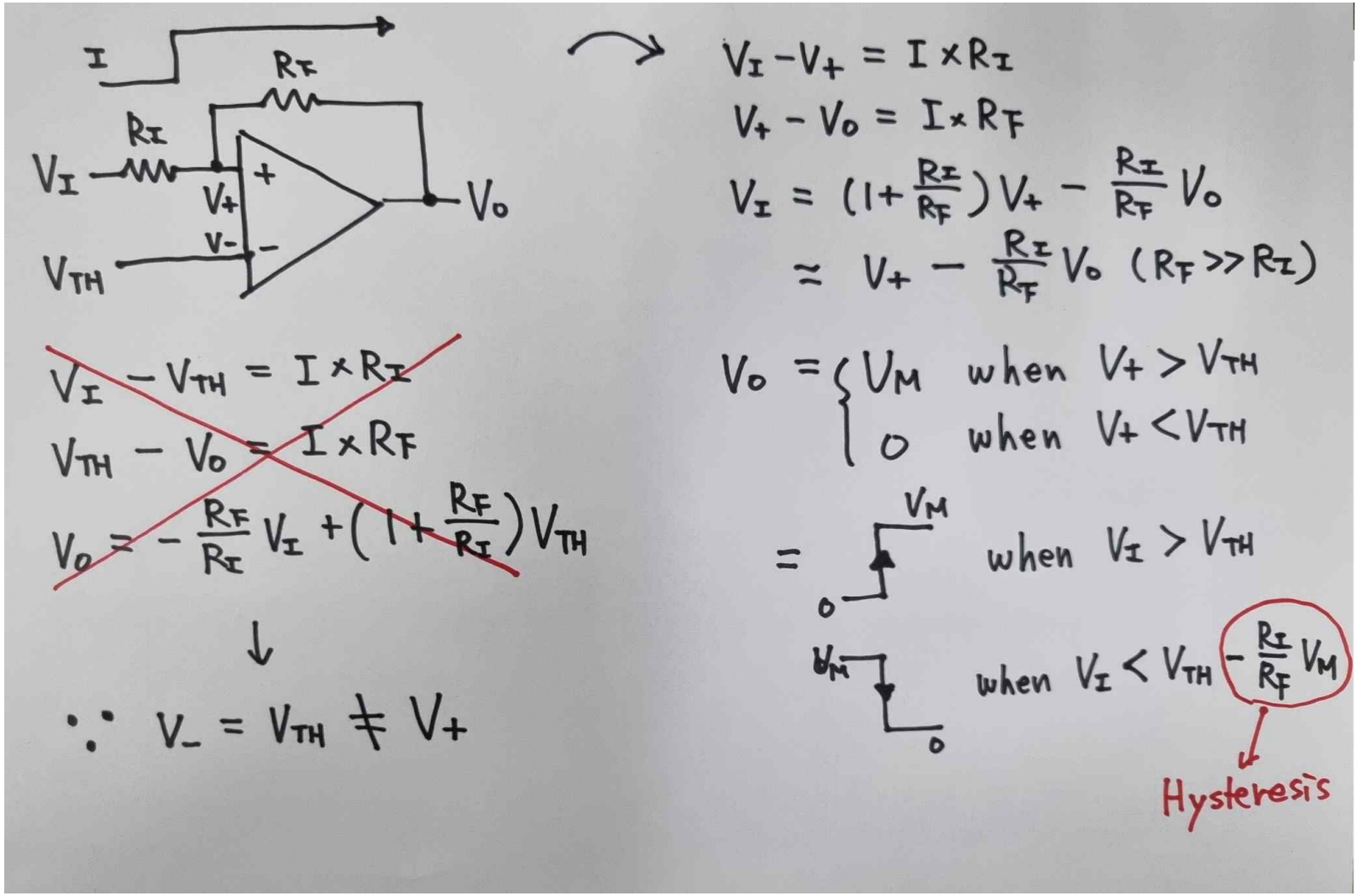


High Pass Filter

Example of Shaping Amplifier : next to Charge sensitive preamplifier

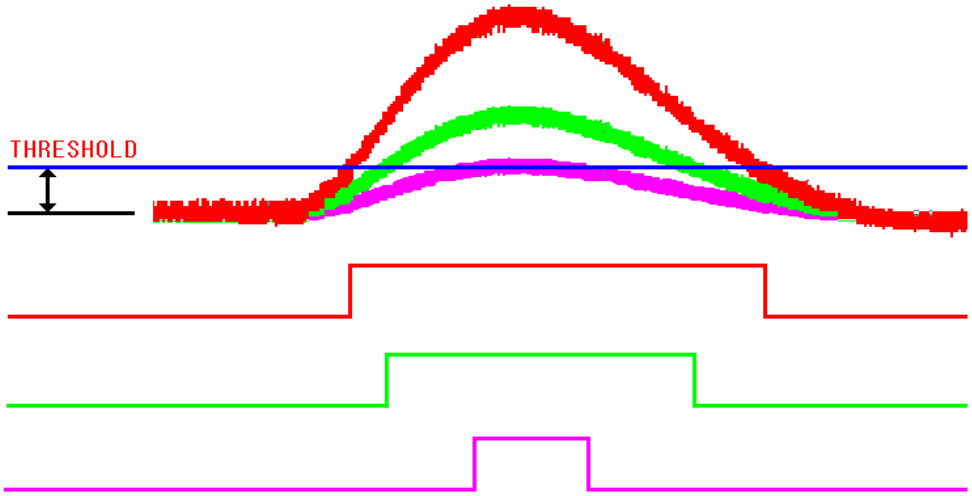


Voltage Comparator



Discriminator

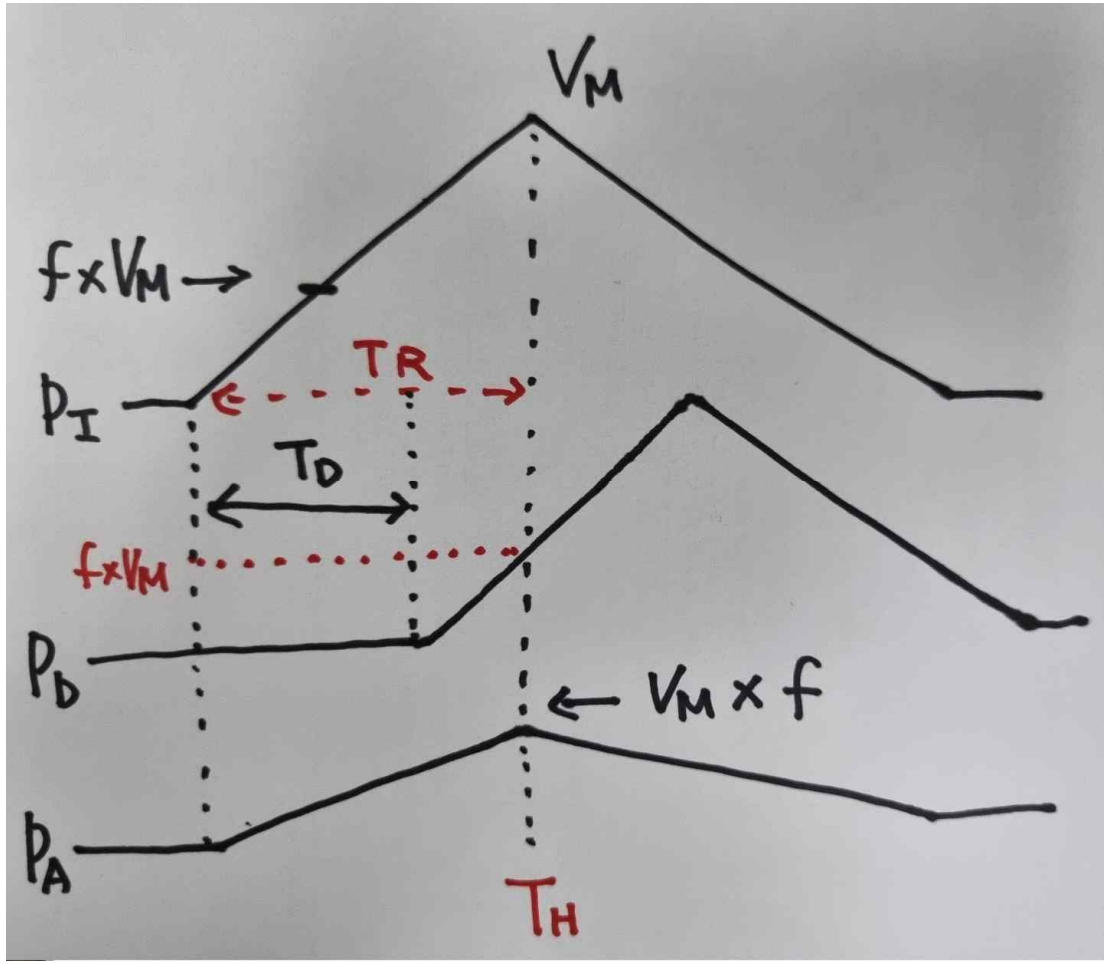
1. To discriminate noise
2. To get pulse timing



Leading edge discriminator

1. Simple
2. Large time walk

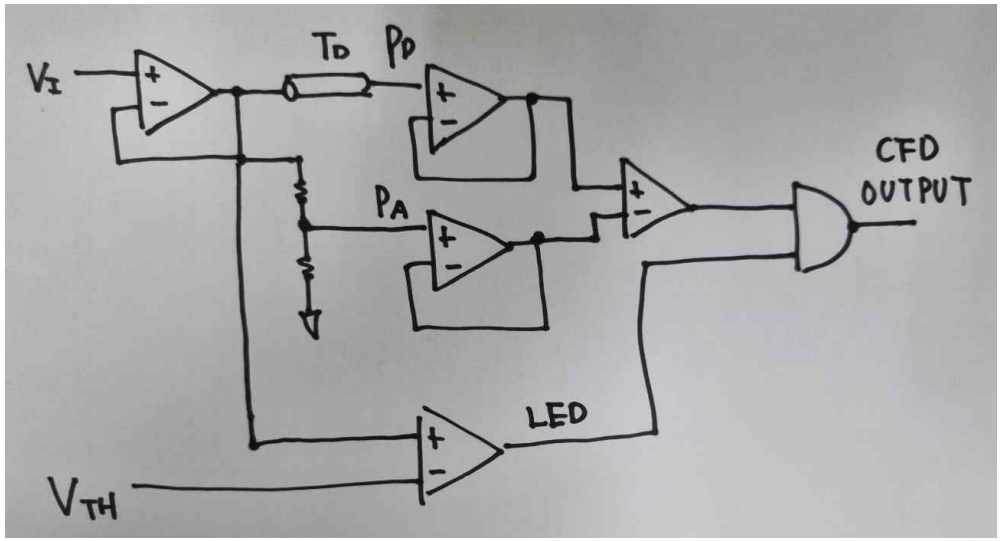
Constant Fraction Discriminator



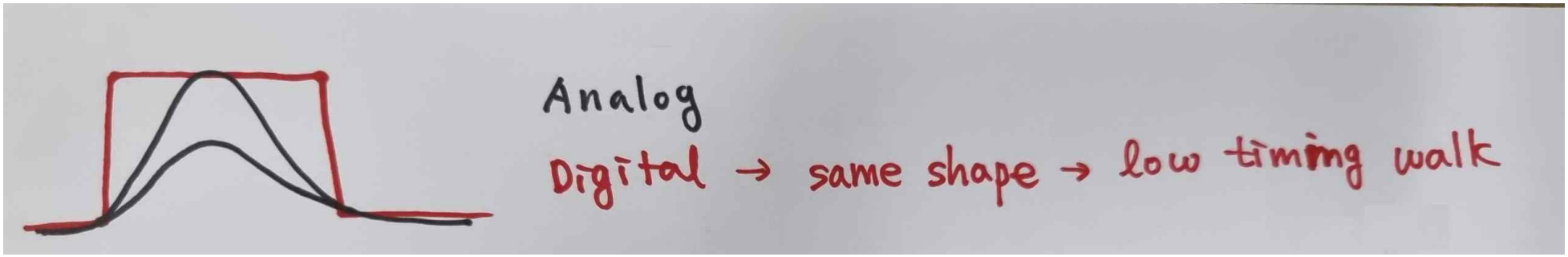
Input pulse is fan out to
- Pd : Delayed (by 1 – f x Tr)
- Pa : Attenuated (by f)

Then Pd and Pa have same Voltage @ Th

Pd has voltage f x Vm @ Th

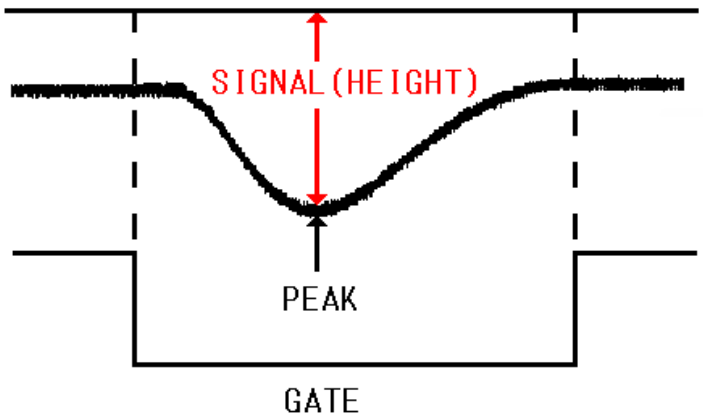


Logic(or Digital) Signal

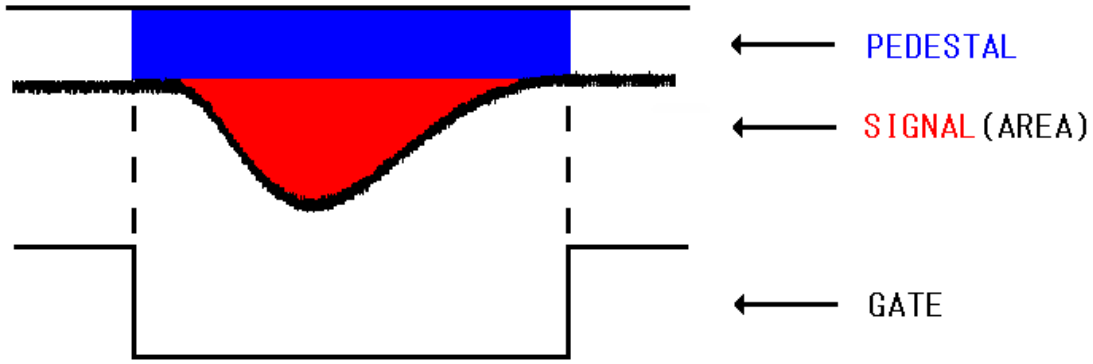


	Type	Low (0)	High (1)
TTL/LVTTL	Single ended	< 0.8 V	> 2.0 V
NIM(slow)	Single ended	< 1.5 V	> 3.0 V
NIM(fast)	Single ended	> -200 mV(-4 mA)	< -600 mV(-12 mA)
ECL	Differential	< -1.48 V	> -0.81 V
LVDS	Differential	< 1.0 V	> 1.4 V

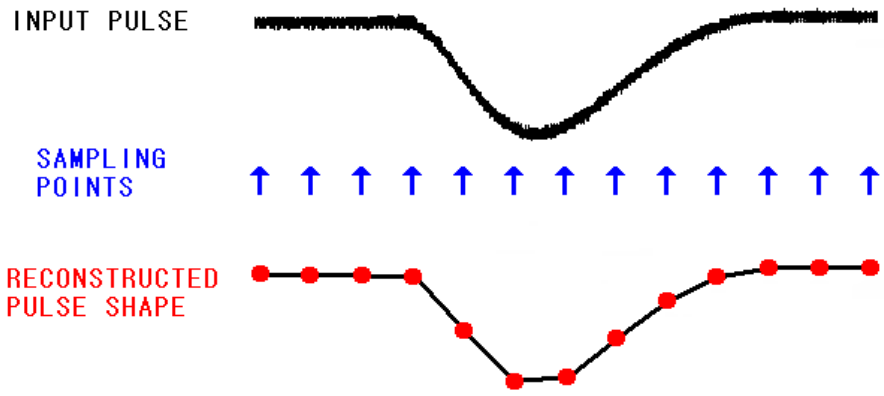
Analog to Digital Converter(ADC)



Peak sensing ADC

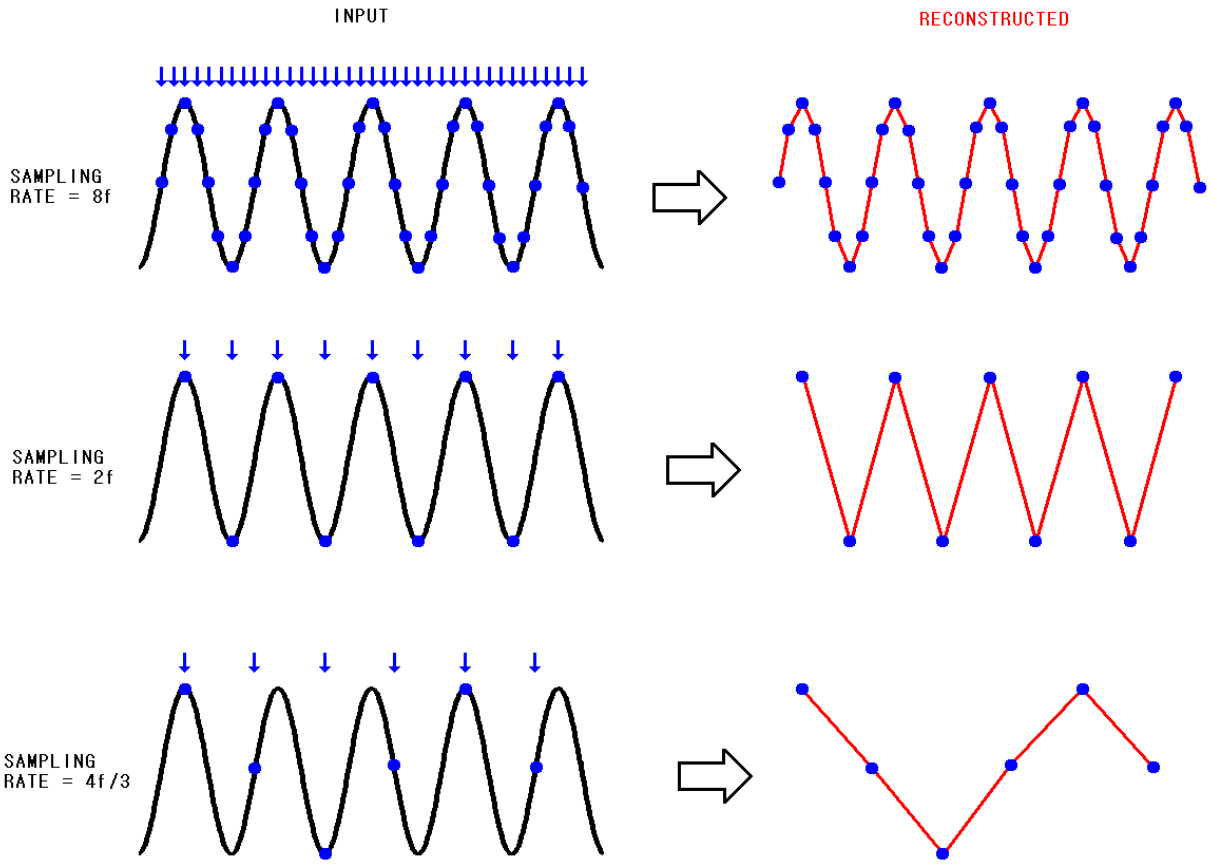


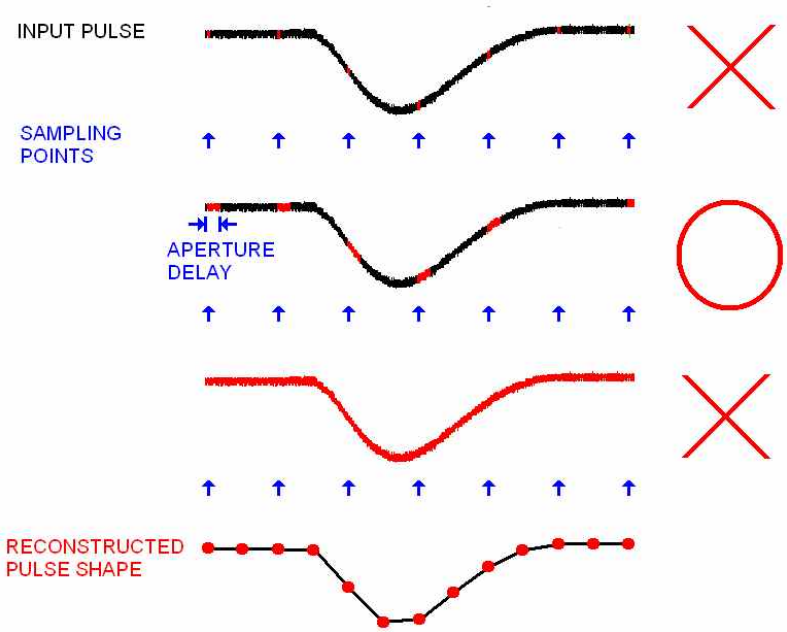
Charge sensing ADC



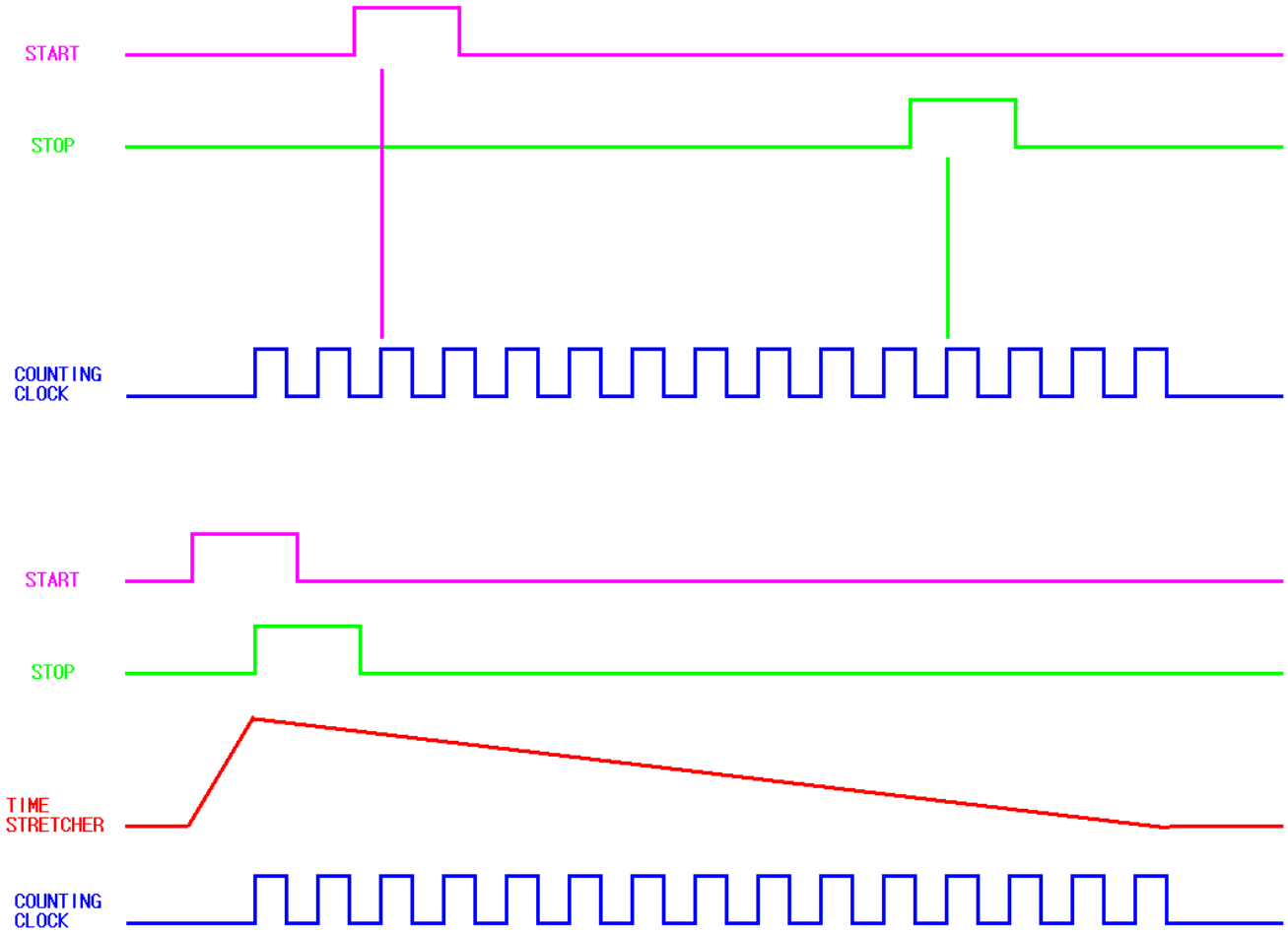
Flash ADC

ADC sampling





Time to Digital Converter(TDC)



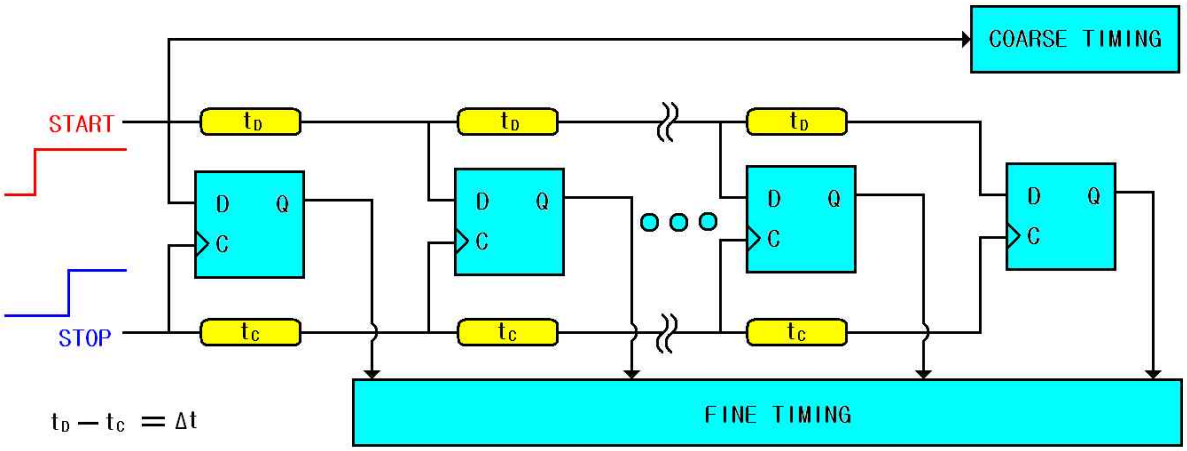
Direct counting

Resolution ~ 1 ns

Time stretching

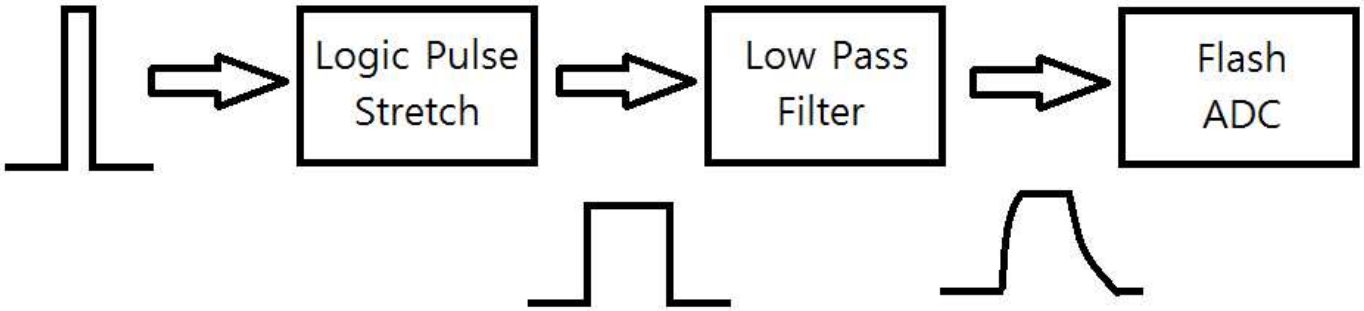
Resolution ~ 10 ps

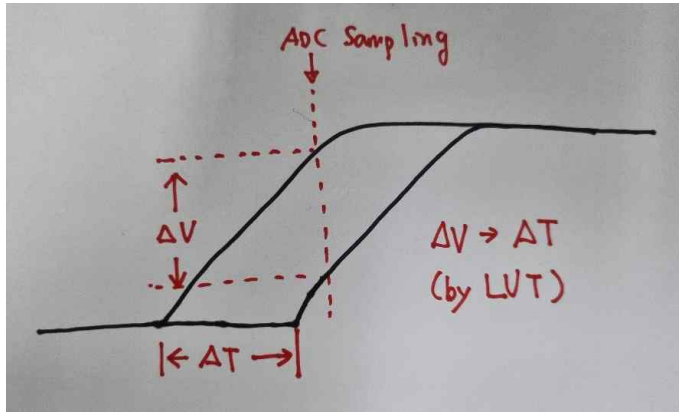
Time to Digital Converter



Time interpolation

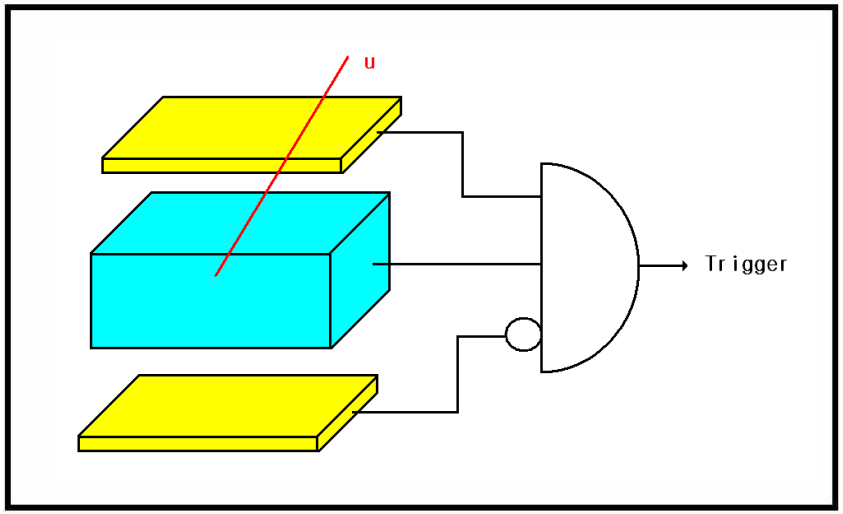
Resolution ~ 10 ps
Multi-hit TDC

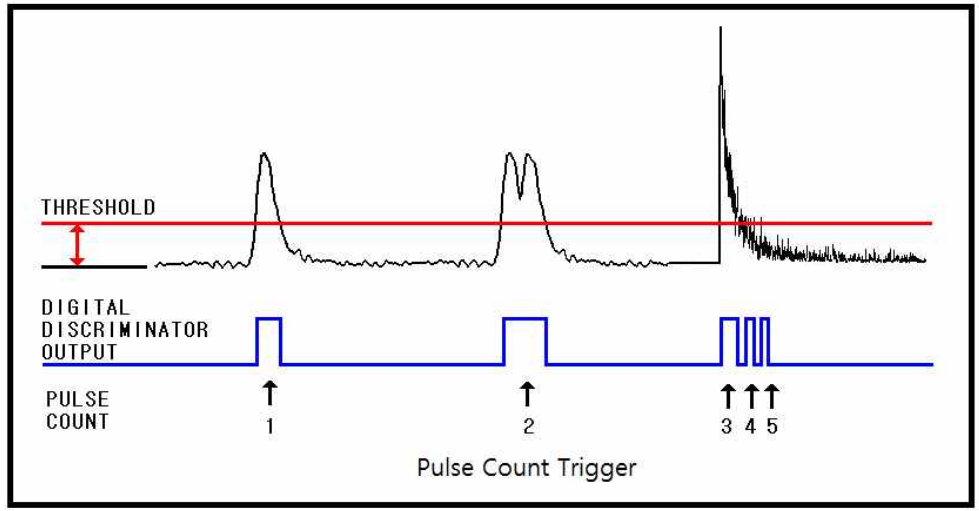


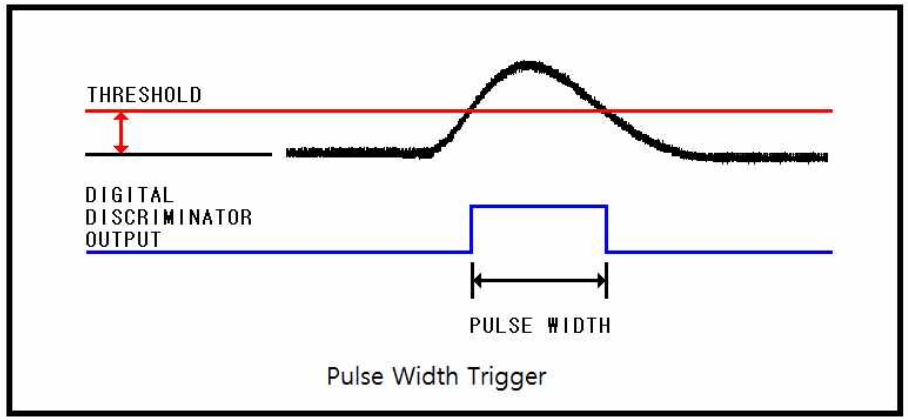


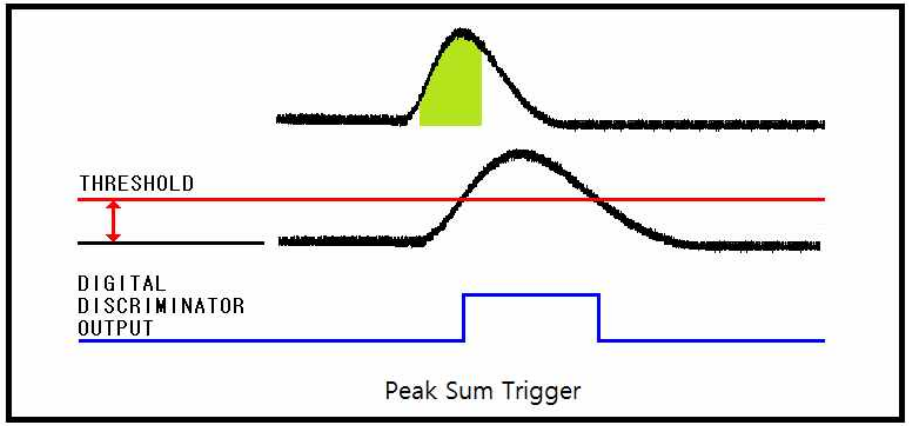
Pulse shaping TDC : resolution ~ 10 ps, multi-hit

Trigger

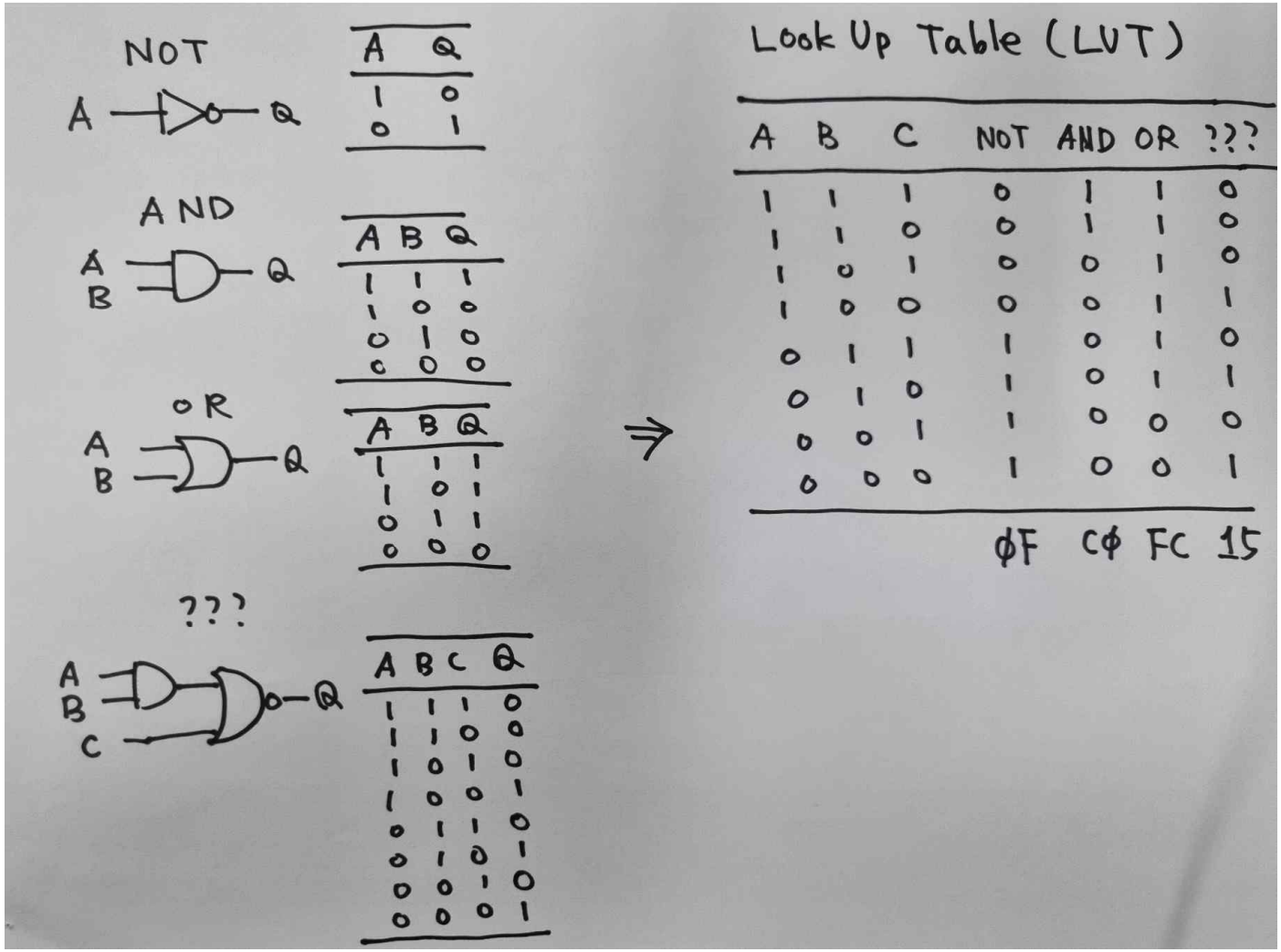

u
Trigger


THRESHOLD
DIGITAL
DISCRIMINATOR
OUTPUT
PULSE
COUNT
1
2
3 4 5
Pulse Count Trigger

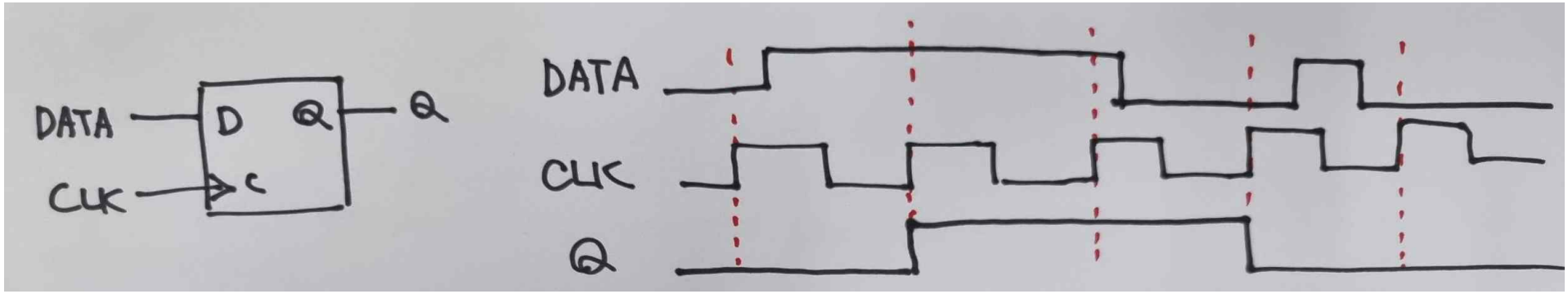

THRESHOLD
DIGITAL
DISCRIMINATOR
OUTPUT
PULSE WIDTH
Pulse Width Trigger

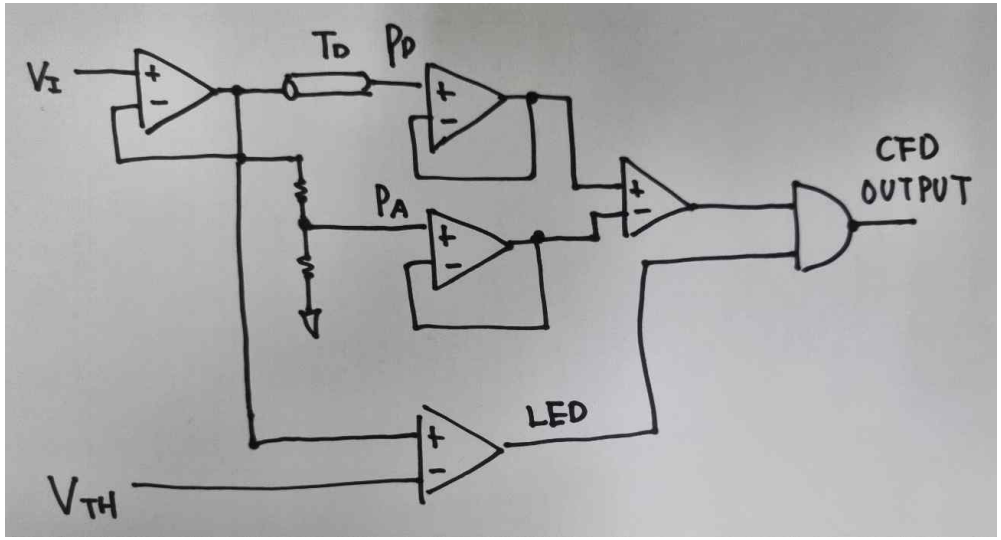

THRESHOLD
DIGITAL
DISCRIMINATOR
OUTPUT
Peak Sum Trigger

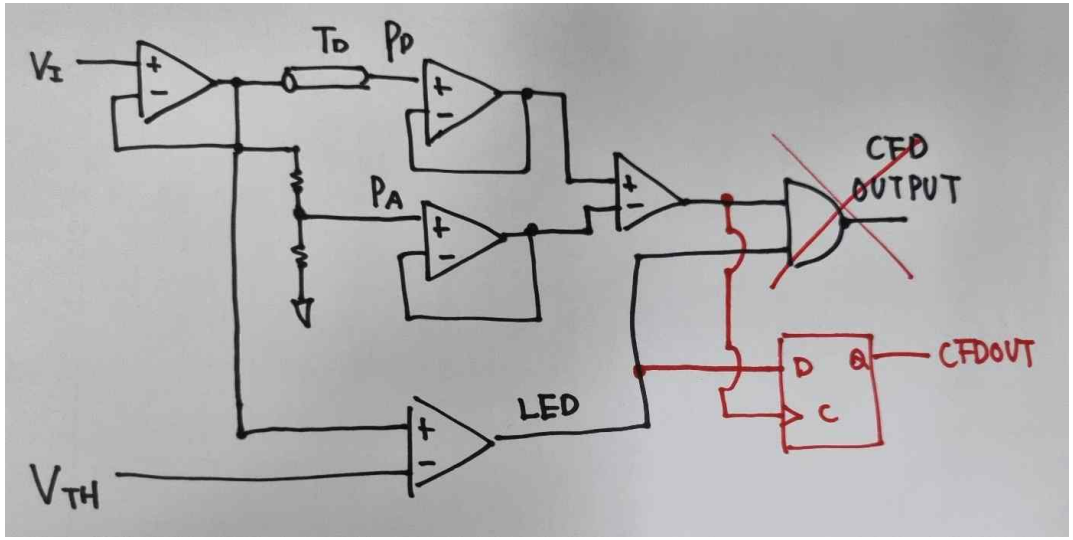
Combinational Logic



Sequential Logic



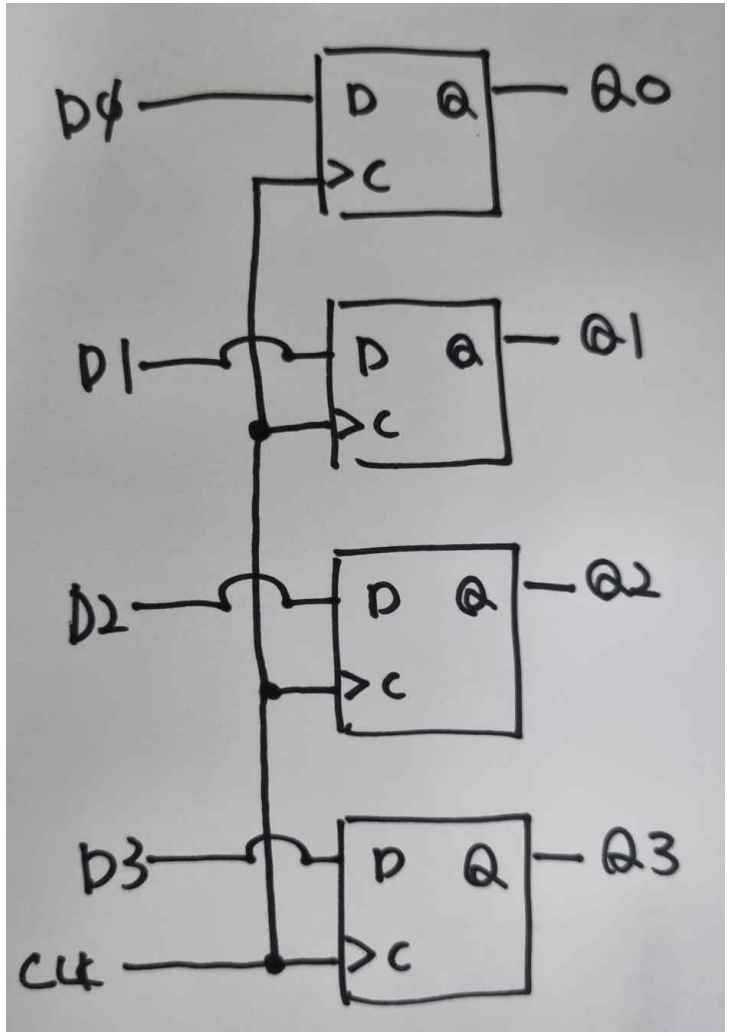




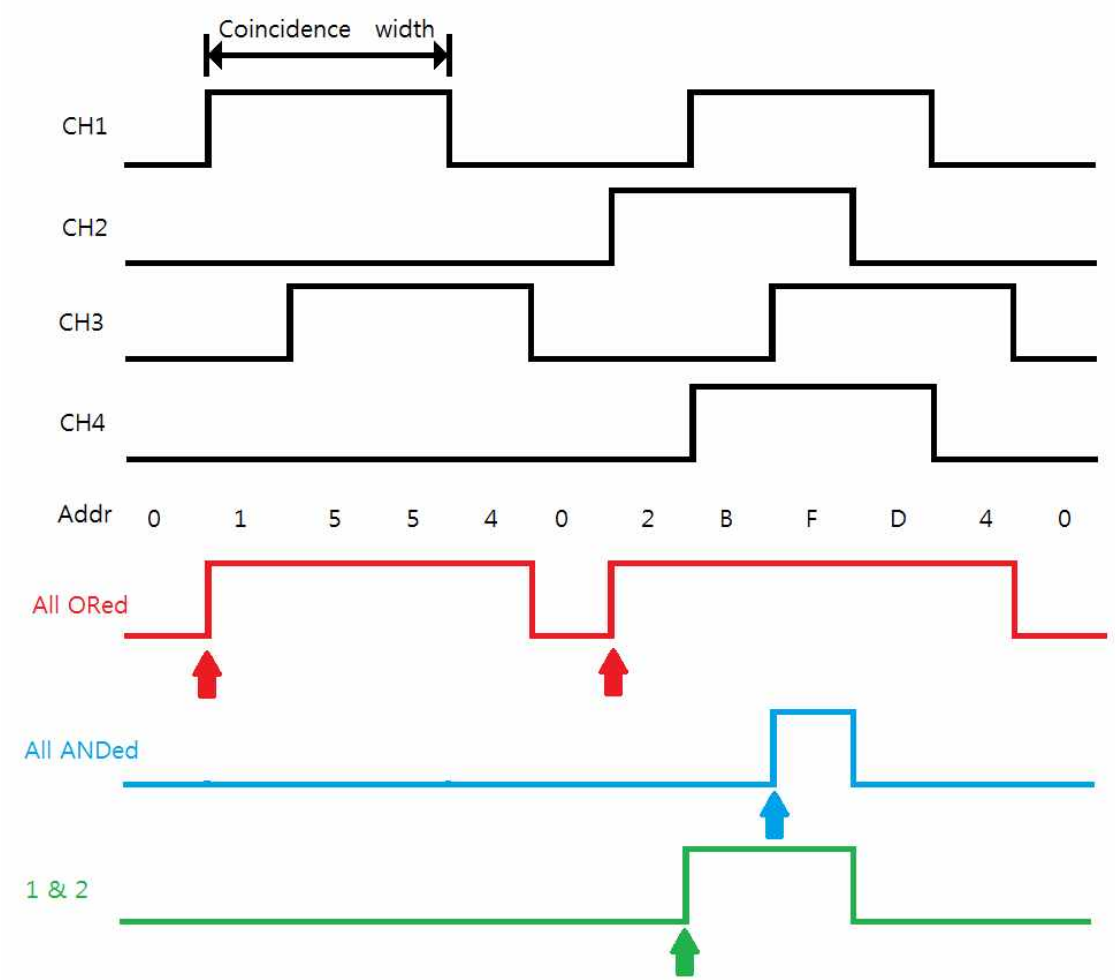
Examples of Sequential Logic

Q0	Q1	Q2	Q3	D3	D2	D1	D0
1	1	1	1	0	0	0	0
1	1	1	0	1	1	1	1
1	1	0	1	1	1	1	0
1	1	0	0	1	1	0	1
1	0	1	1	1	1	0	0
1	0	1	0	1	0	1	1
1	0	0	1	1	0	1	0
1	0	0	0	1	0	0	1
0	1	1	1	1	0	0	0
0	1	1	0	0	1	1	1
0	1	0	1	0	1	1	0
0	1	0	0	0	1	0	1
0	0	1	1	0	1	0	0
0	0	1	0	0	0	1	1
0	0	0	1	0	0	1	0
0	0	0	0	0	0	0	1

Q0	Q1	Q2	Q3	D3	D2	D1	D0
1	1	1	1	0	0	0	0
1	1	1	0	0	0	0	0
1	1	0	1	0	0	0	0
1	1	0	0	0	0	0	0
1	0	1	1	0	0	0	0
1	0	1	0	0	0	0	0
1	0	0	1	0	0	0	0
1	0	0	0	1	0	0	1
0	1	1	1	1	0	0	0
0	1	1	0	0	1	1	1
0	1	0	1	0	1	1	0
0	1	0	0	0	1	0	1
0	0	1	1	0	1	0	0
0	0	1	0	0	0	1	1
0	0	0	1	0	0	1	0
0	0	0	0	0	0	0	1



Trigger by combination



Trigger Lookup Table

CH 4 3 2 1	Addr	All ORed	All ANDed	1 & 2
1 1 1 1	F	1	1	1
1 1 1 0	E	1	0	0
1 1 0 1	D	1	0	0
1 1 0 0	C	1	0	0
1 0 1 1	B	1	0	1
1 0 1 0	A	1	0	0
1 0 0 1	9	1	0	0
1 0 0 0	8	1	0	0
0 1 1 1	7	1	0	1
0 1 1 0	6	1	0	0
0 1 0 1	5	1	0	0
0 1 0 0	4	1	0	0
0 0 1 1	3	1	0	1
0 0 1 0	2	1	0	0
0 0 0 1	1	1	0	0
0 0 0 0	0	0	0	0
		0xFFFE	0x8000	0x8888

Data Acquisition

CAMAC

VME

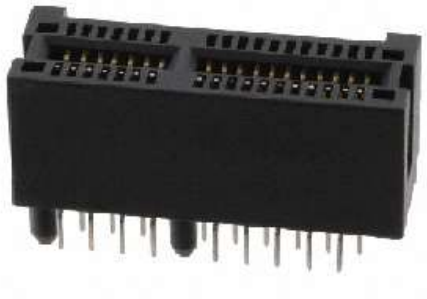
Standard

Custom

Data Acquisition

Ethernet : 125 MB/s max, ~30 MB/s typically

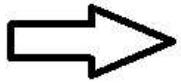
USB : 500 MB/s max, ~100 MB/s typically

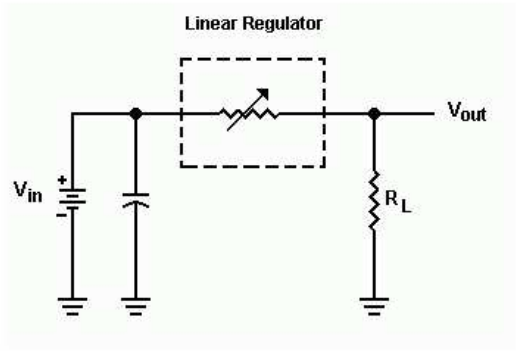


PCI : 63 GB/s max, ~??? typically

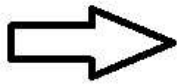
Power Supply

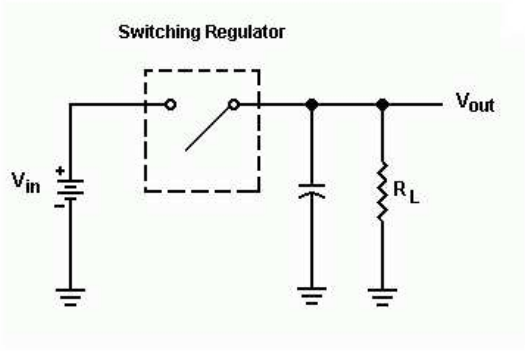
Linear



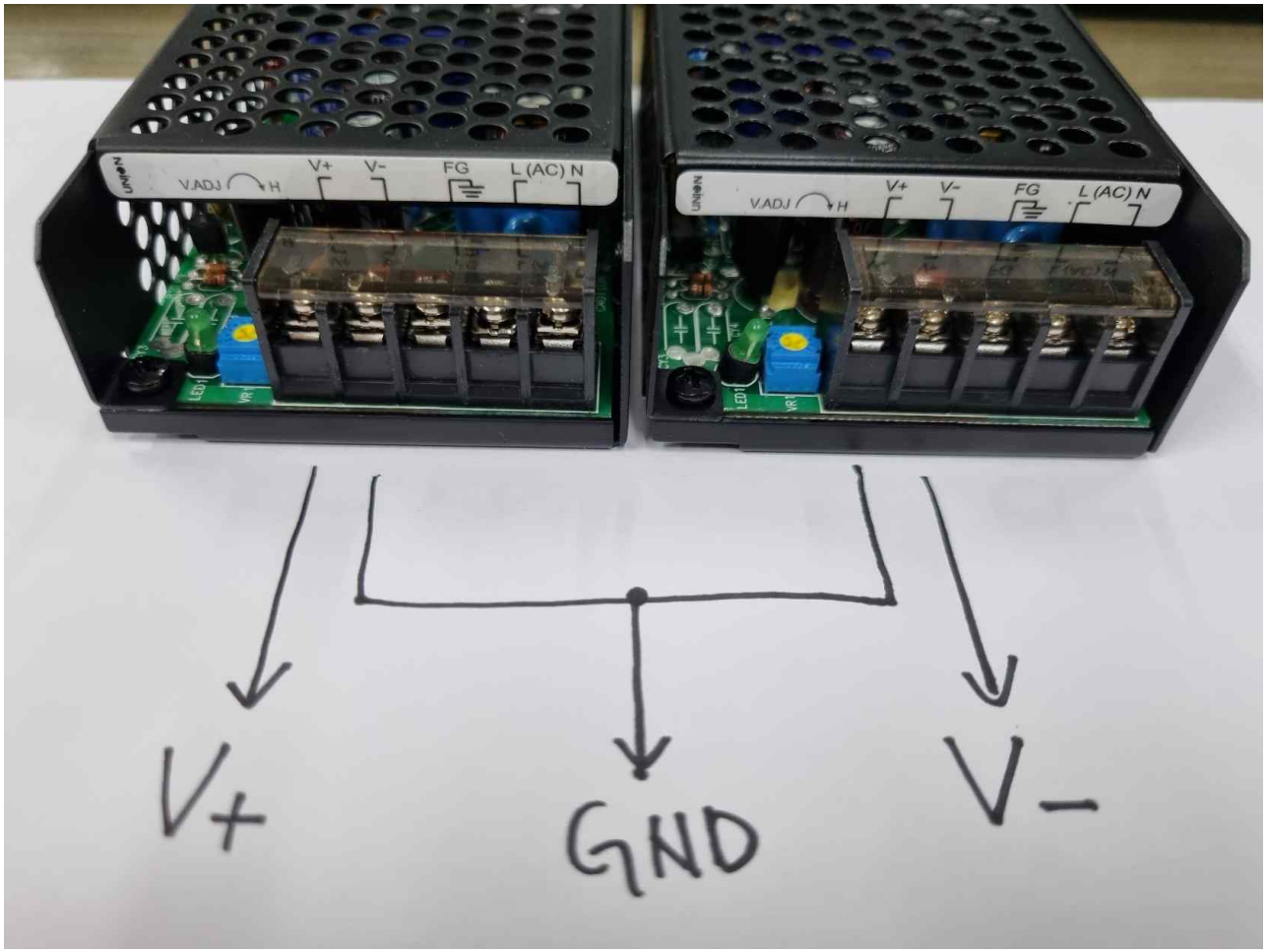


Switching





Power Supply Example



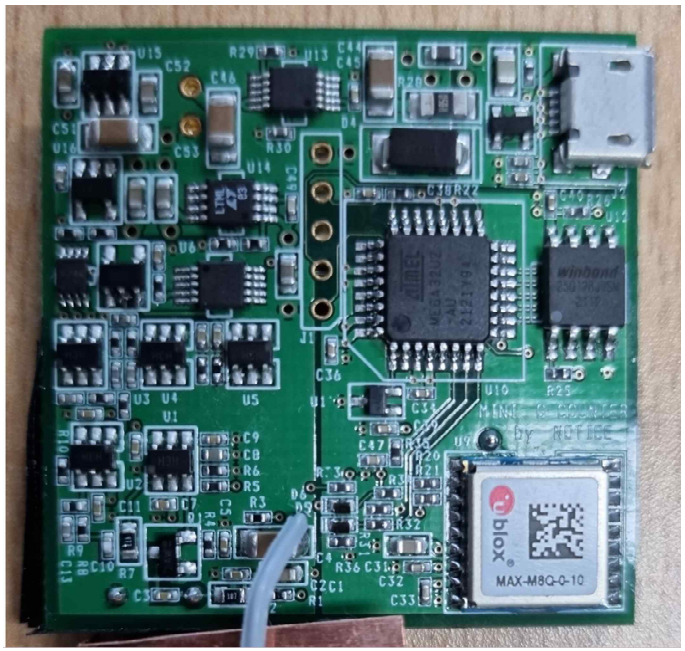
1. L, N to

2. FG to GND

3. Check FG & V-
   are not shorted

4. Variation :
   V- to GND
   GND to V1
   V+ to V1 + V2
   even if V1 is HV!

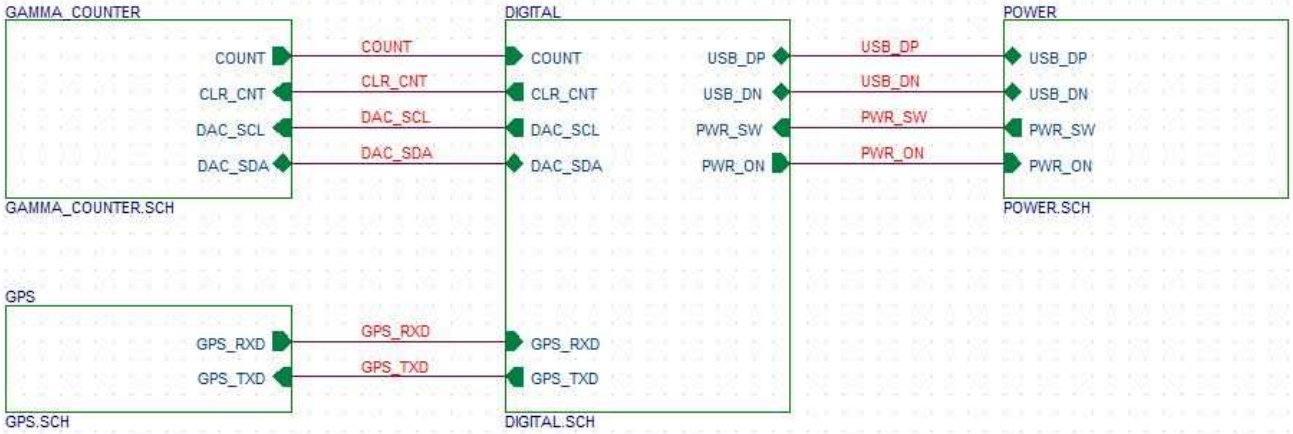
Example of electronics board : Gamma ray counter board



1. Pin PD to detect Gamma ray directly
2. Charge sensitive preamplifier
3. CR-RC2 shaping amplifier
4. Leading edge discriminator
5. MCU for counting logic
6. USB2 interface
7. GPS

Electronics board manufacturing process

1. Conceptual design and colleting parts
2. Draw schematics
3. Draw Printed Circuit Board(PCB) layout
4. Solder and assemble parts on PCB
5. Write Firmware(MCU, FPGA …)
6. Write Software
7. Test and Debug



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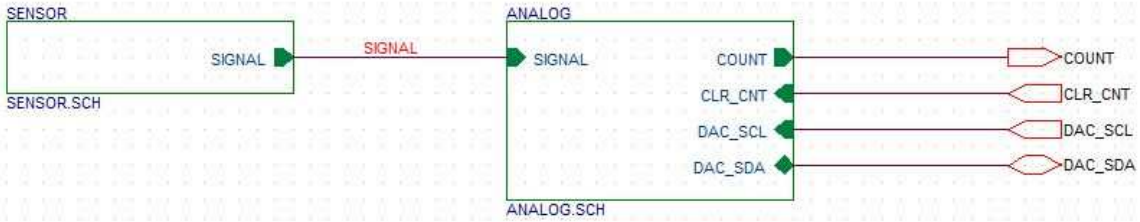
Size: A	Document Number: <Doc>		Rev: 1.0
Date: Friday, August 06, 2021	Sheet 1 of 1		



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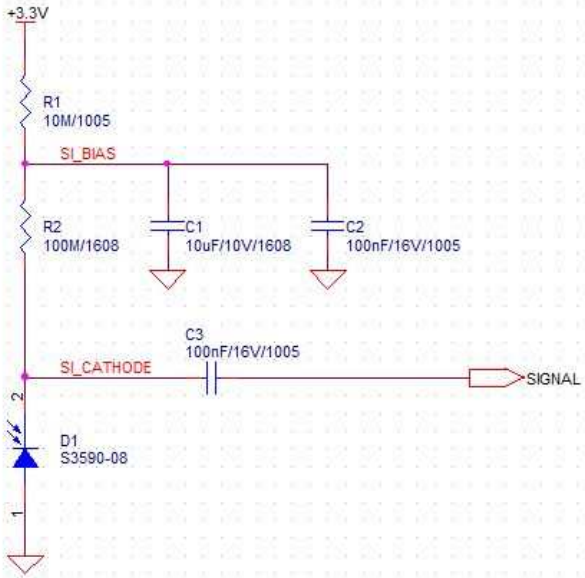
Date: Friday, August 06, 2021	Sheet 1 of 1	



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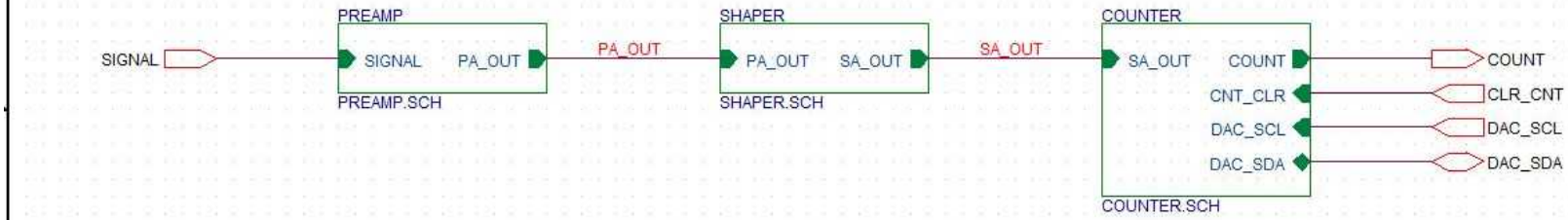

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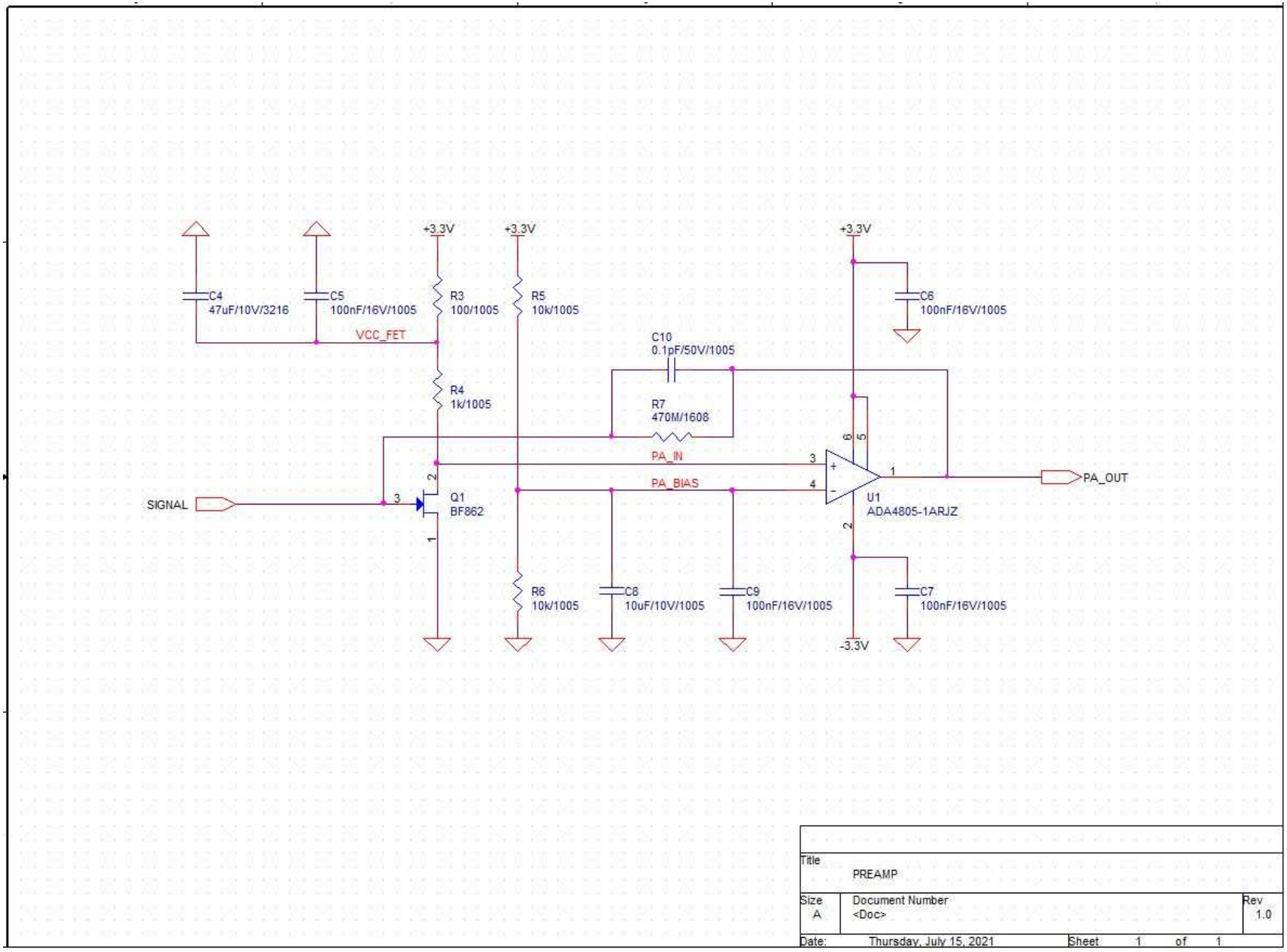
+3.3V
+3.3V
+3.3V
C4
47uF/10V/3216
C5
100nF/16V/1005
R3
100/1005
R5
10k/1005
C6
100nF/16V/1005
VCC_FET
C10
0.1pF/50V/1005
R4
1k/1005
R7
470M/1608
PA_IN
PA_BIAS
SIGNAL
Q1
BF862
U1
ADA4805-1ARJZ
PA_OUT
R6
10k/1005
C8
10uF/10V/1005
C9
100nF/16V/1005
C7
100nF/16V/1005
-3.3V
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PREAMP
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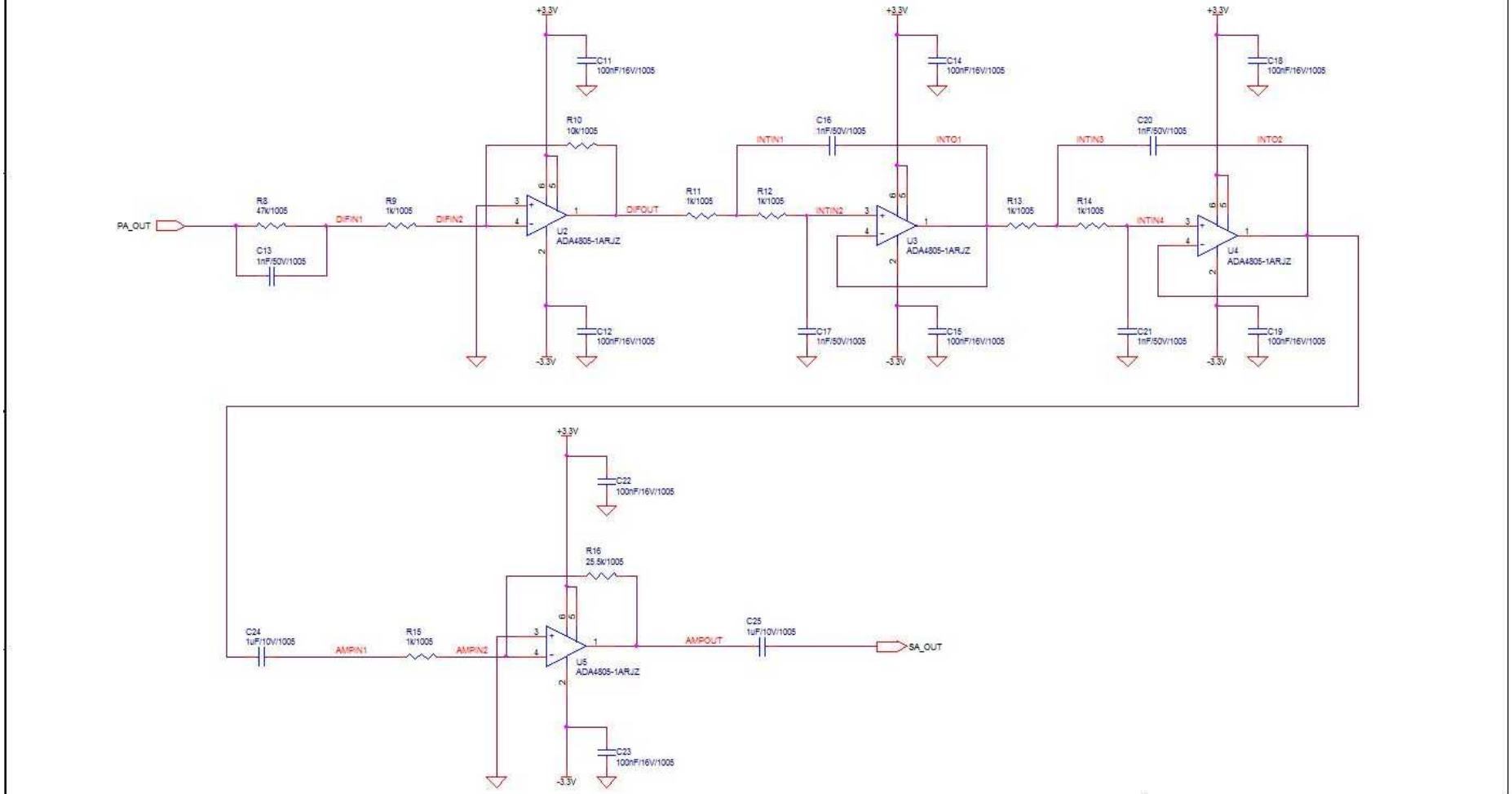

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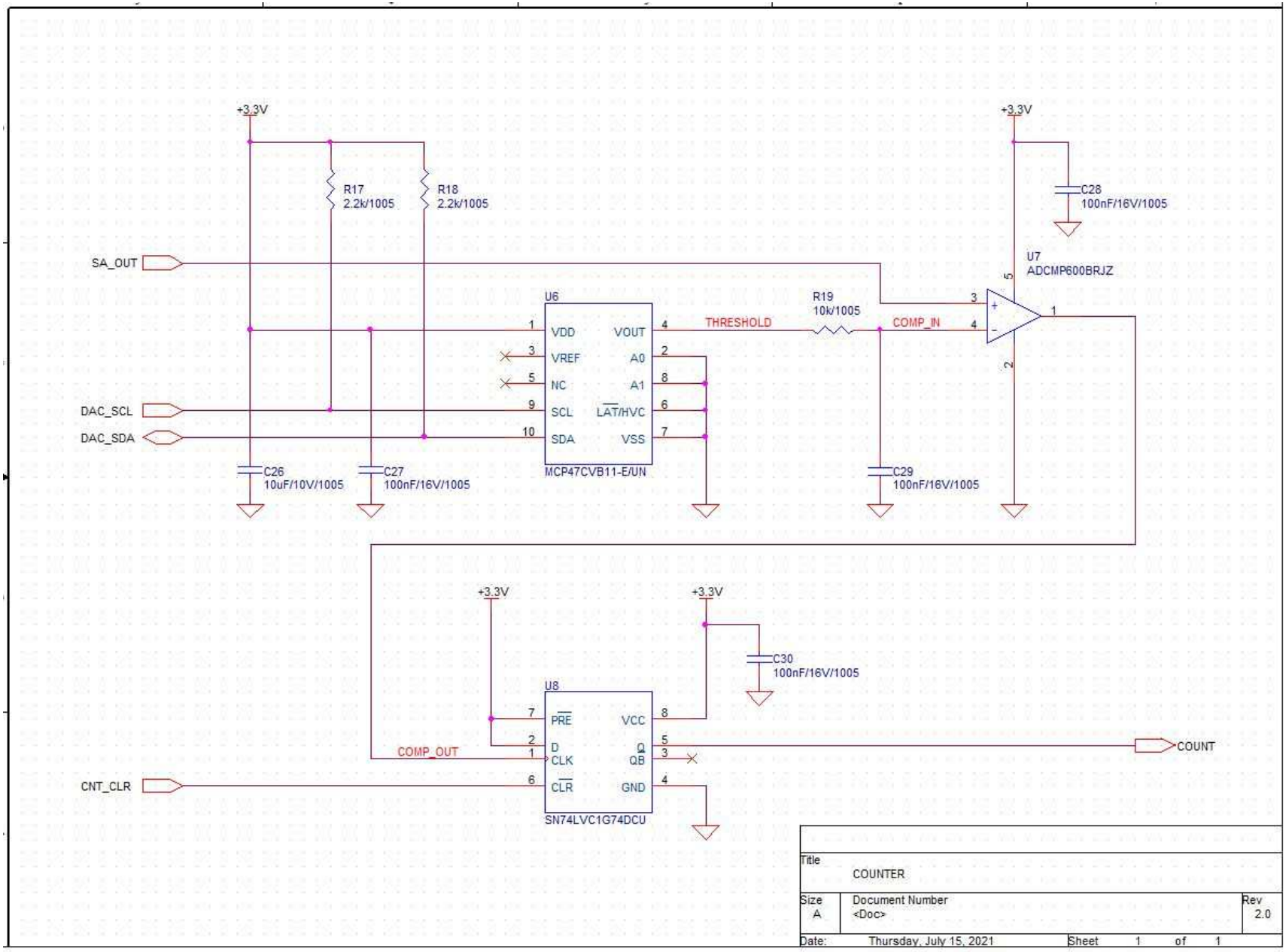
Size B	Document Number <Doc>	Rev 1.0
Date: Thursday, July 15, 2021	Sheet 1 of 1	


+3.3V
R17
2.2k/1005
R18
2.2k/1005
SA_OUT
DAC_SCL
DAC_SDA
U6
VDD
VREF
NC
SCL
SDA
VOUT
A0
A1
LAT/HVC
VSS
MCP47CVB11-E/UN
THRESHOLD
R19
10k/1005
COMP_IN
+3.3V
C28
100nF/16V/1005
U7
ADCMP600BRJZ
C26
10uF/10V/1005
C27
100nF/16V/1005
C29
100nF/16V/1005
+3.3V
+3.3V
C30
100nF/16V/1005
U8
PRE
D
CLK
CLR
VCC
Q
QB
GND
SN74LVC1G74DCU
COMP_OUT
CNT_CLR
COUNT
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COUNTER
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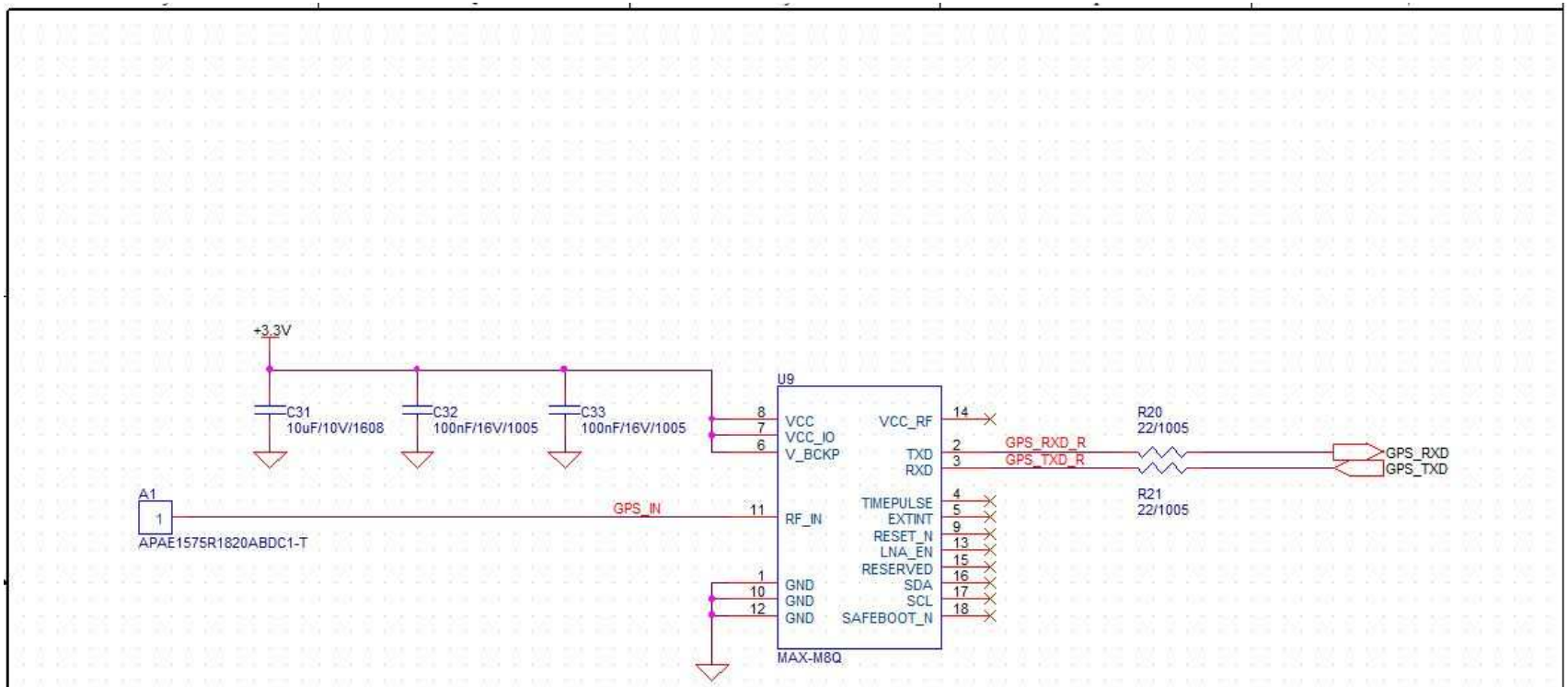

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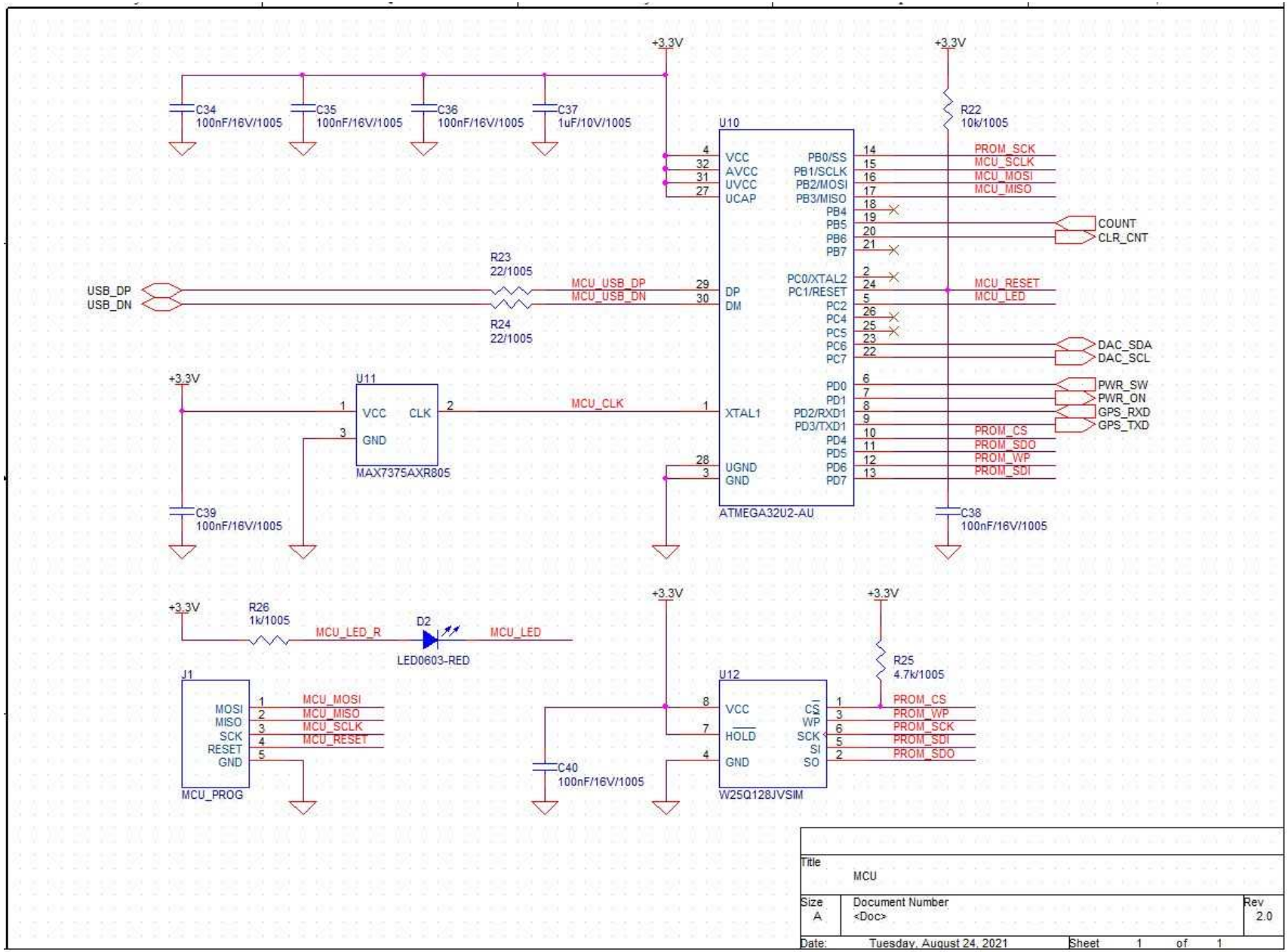
+3.3V
C34
100nF/16V/1005
C35
100nF/16V/1005
C36
100nF/16V/1005
C37
1uF/10V/1005
U10
VCC
AVCC
UVCC
UCAP
PB0/SS
PB1/SCLK
PB2/MOSI
PB3/MISO
PB4
PB5
PB6
PB7
PC0/XTAL2
PC1/RESET
PC2
PC4
PC5
PC6
PC7
PD0
PD1
PD2/RXD1
PD3/TXD1
PD4
PD5
PD6
PD7
XTAL1
UGND
GND
ATMEGA32U2-AU
R22
10k/1005
PROM_SCK
MCU_SCLK
MCU_MOSI
MCU_MISO
COUNT
CLR_CNT
MCU_RESET
MCU_LED
DAC_SDA
DAC_SCL
PWR_SW
PWR_ON
GPS_RXD
GPS_TXD
PROM_CS
PROM_SDO
PROM_WP
PROM_SDI
R23
22/1005
R24
22/1005
USB_DP
USB_DN
MCU_USB_DP
MCU_USB_DN
U11
VCC
CLK
GND
MAX7375AXR805
MCU_CLK
C38
100nF/16V/1005
C39
100nF/16V/1005
R26
1k/1005
MCU_LED_R
D2
LED0603-RED
J1
MOSI
MISO
SCK
RESET
GND
MCU_PROG
MCU_MOSI
MCU_MISO
MCU_SCLK
MCU_RESET
U12
VCC
HOLD
GND
CS
WP
SCK
SI
SO
W25Q128JVSIM
R25
4.7k/1005
C40
100nF/16V/1005
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MCU
Size
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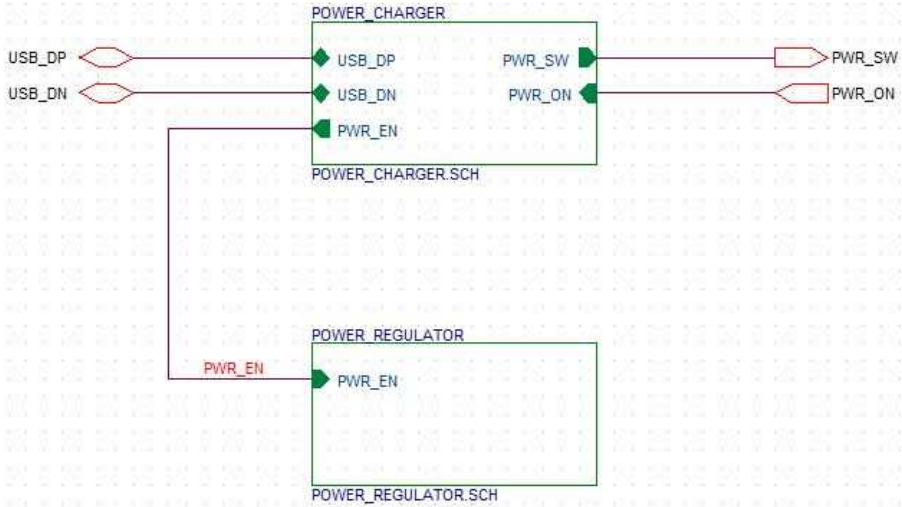

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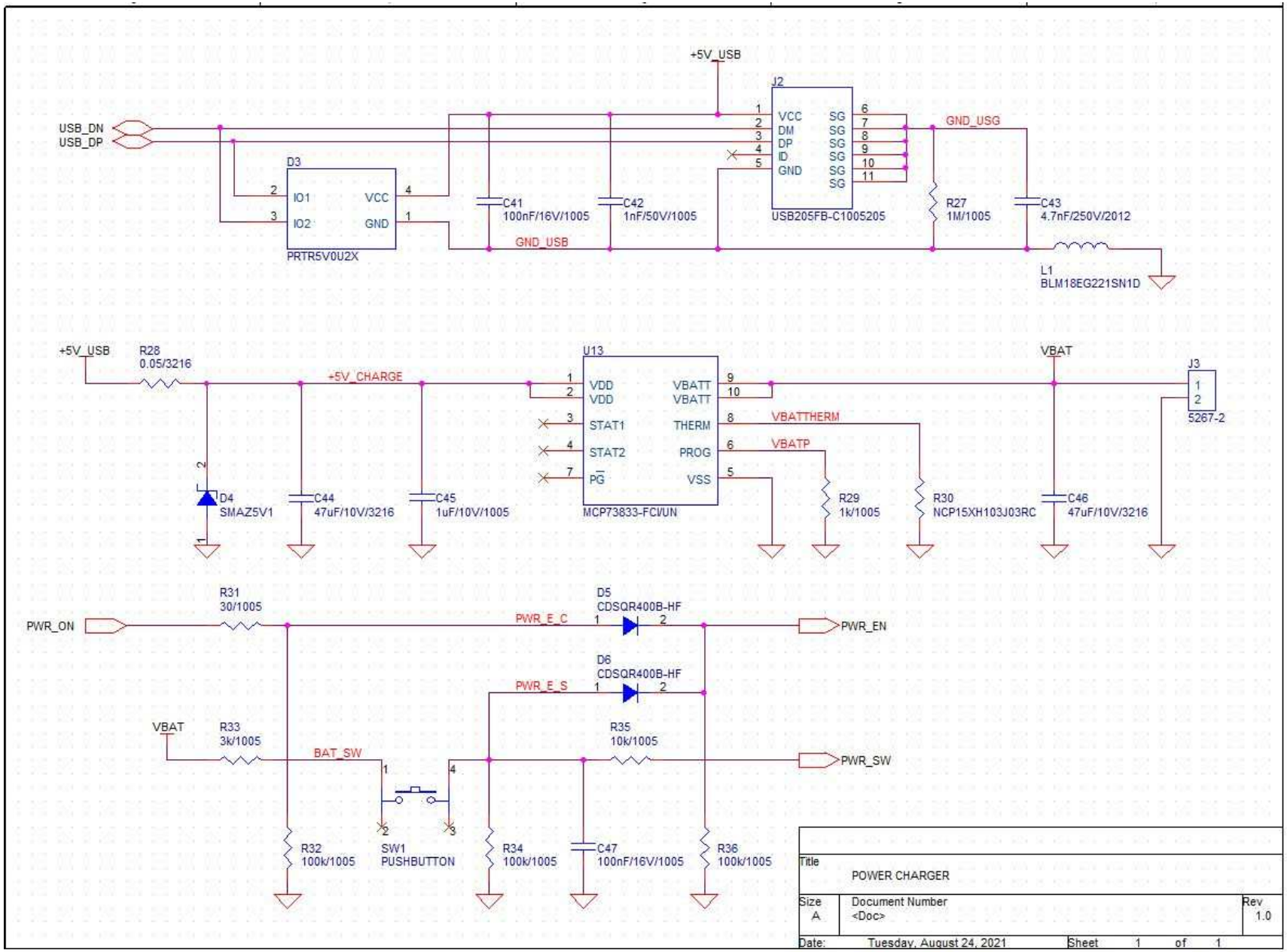
Date: Friday, August 06, 2021	Sheet 1 of 1	


+5V_USB
J2
USB_DN
USB_DP
VCC
DM
DP
ID
GND
SG
GND_USG
USB205FB-C1005205
D3
IO1
IO2
VCC
GND
PRTR5V0U2X
C41
100nF/16V/1005
C42
1nF/50V/1005
GND_USB
R27
1M/1005
C43
4.7nF/250V/2012
L1
BLM18EG221SN1D
+5V_USB
R28
0.05/3216
+5V_CHARGE
U13
VDD
STAT1
STAT2
PG
VBATT
THERM
PROG
VSS
MCP73833-FCI/UN
VBATTHERM
VBATP
VBAT
J3
5267-2
D4
SMAZ5V1
C44
47uF/10V/3216
C45
1uF/10V/1005
R29
1k/1005
R30
NCP15XH103J03RC
C46
47uF/10V/3216
PWR_ON
R31
30/1005
D5
CDSQR400B-HF
PWR_E_C
PWR_EN
D6
CDSQR400B-HF
PWR_E_S
VBAT
R33
3k/1005
BAT_SW
R35
10k/1005
PWR_SW
R32
100k/1005
SW1
PUSHBUTTON
R34
100k/1005
C47
100nF/16V/1005
R36
100k/1005
Title
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Size
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Document Number
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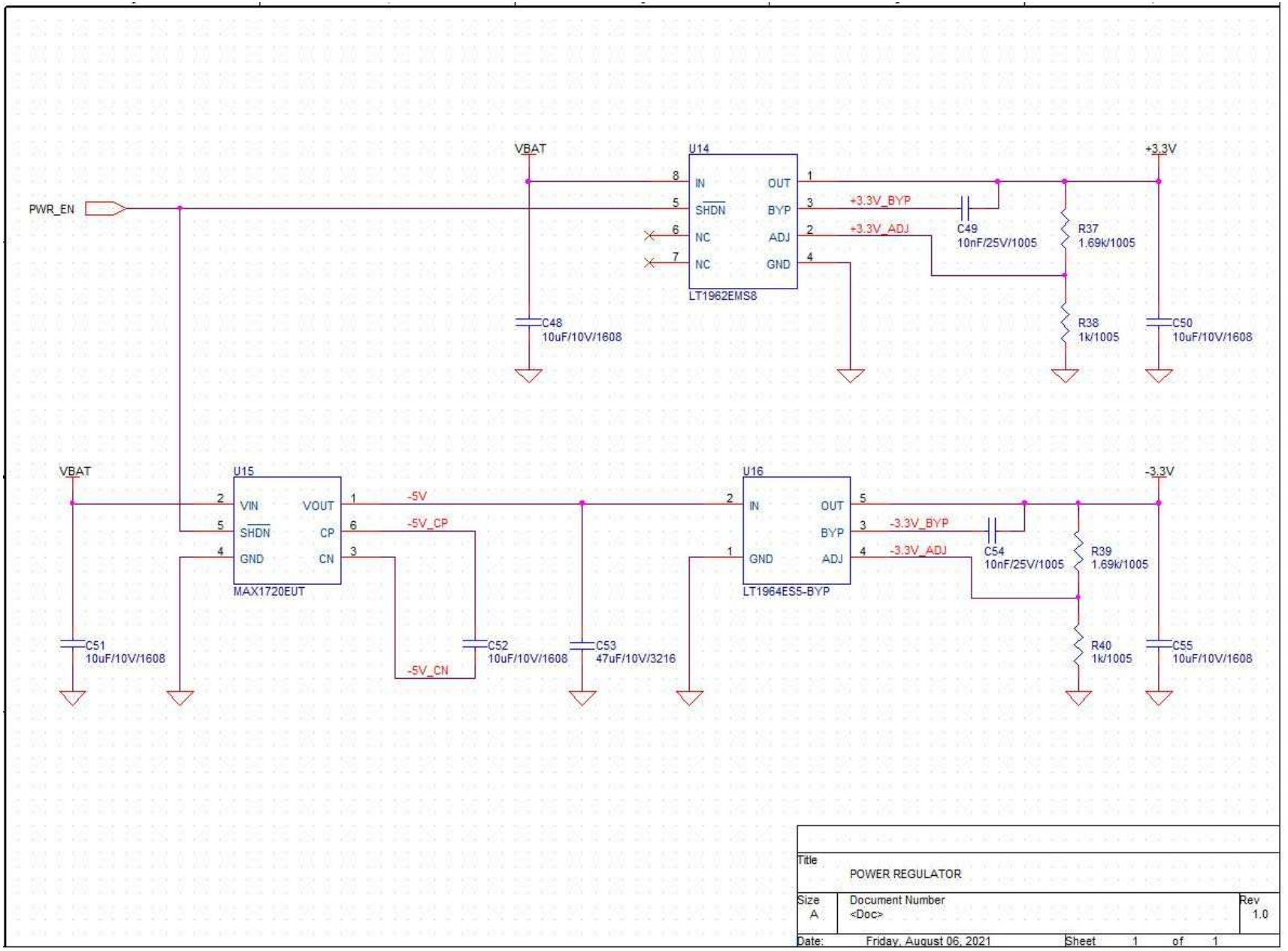
VBAT
U14
+3.3V
PWR_EN
8
IN
OUT
1
5
SHDN
BYP
3
+3.3V_BYP
6
NC
ADJ
2
+3.3V_ADJ
7
NC
GND
4
LT1962EMS8
C49
10nF/25V/1005
R37
1.69k/1005
C48
10uF/10V/1608
R38
1k/1005
C50
10uF/10V/1608
VBAT
U15
U16
-3.3V
2
VIN
VOUT
1
-5V
5
SHDN
CP
6
-5V_CP
4
GND
CN
3
MAX1720EUT
2
IN
OUT
5
BYP
3
-3.3V_BYP
1
GND
ADJ
4
-3.3V_ADJ
LT1964ES5-BYP
C54
10nF/25V/1005
R39
1.69k/1005
C51
10uF/10V/1608
C52
10uF/10V/1608
C53
47uF/10V/3216
-5V_CN
R40
1k/1005
C55
10uF/10V/1608
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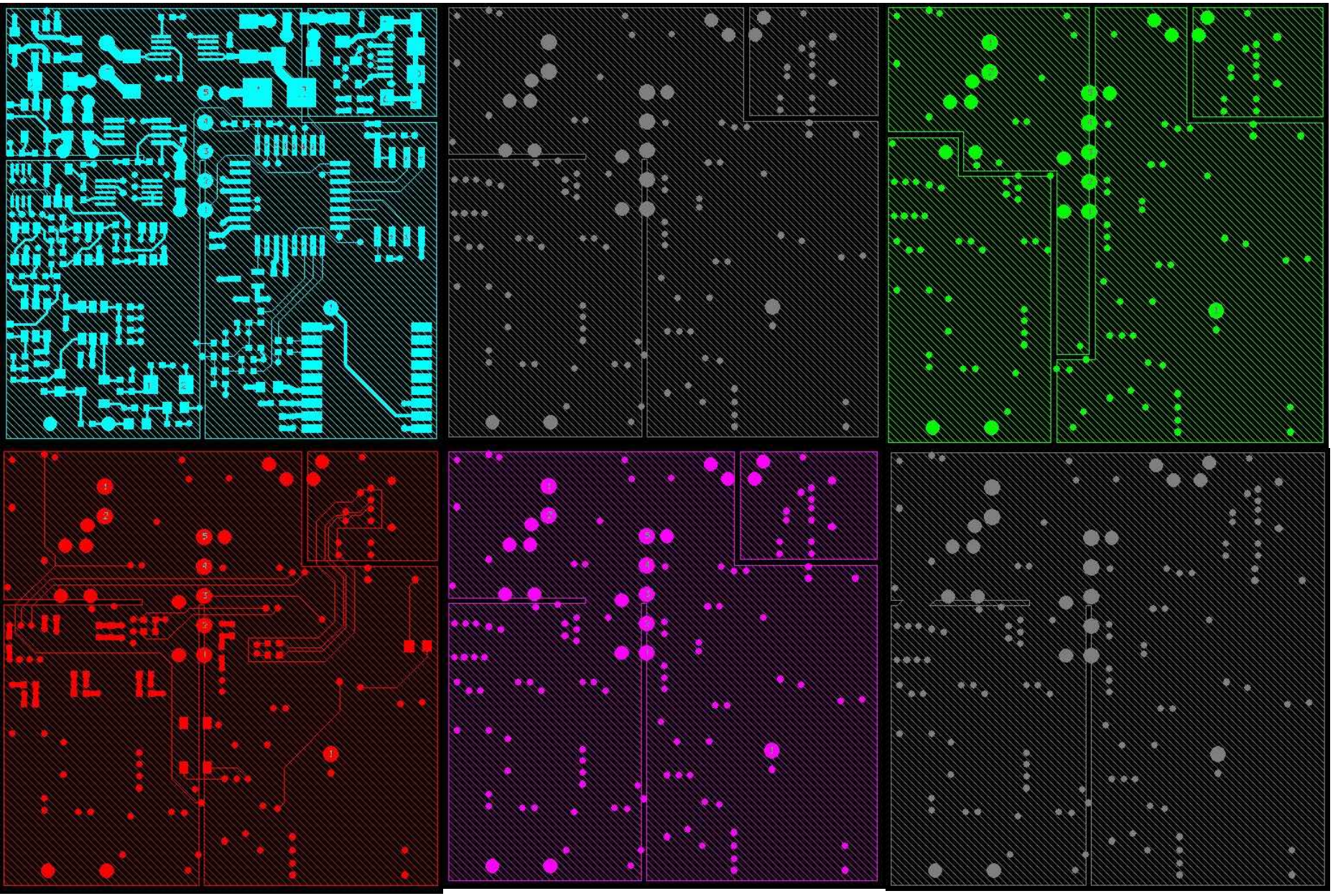

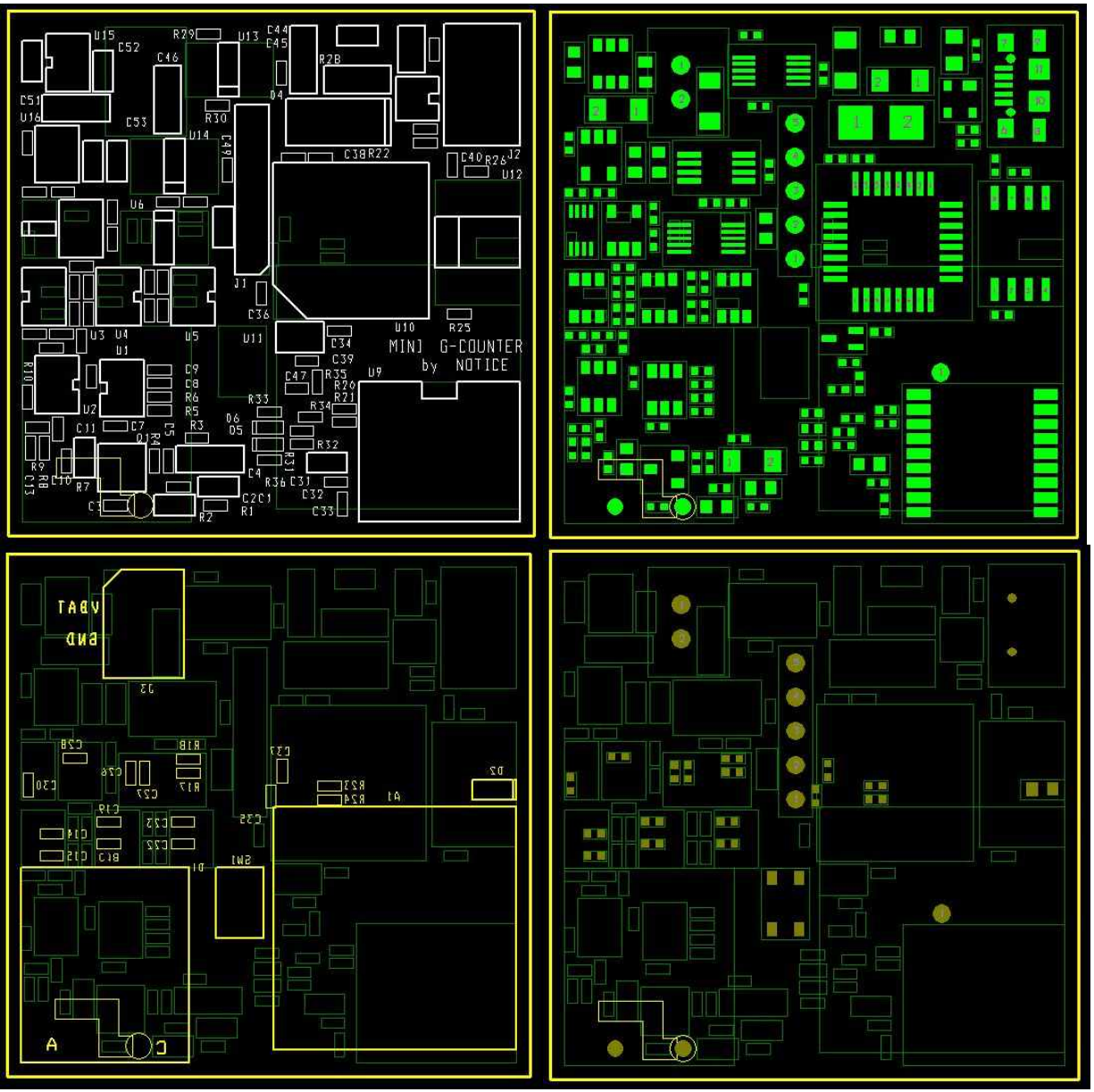
MINI G-COUNTER
by NOTICE
VBAT
GND