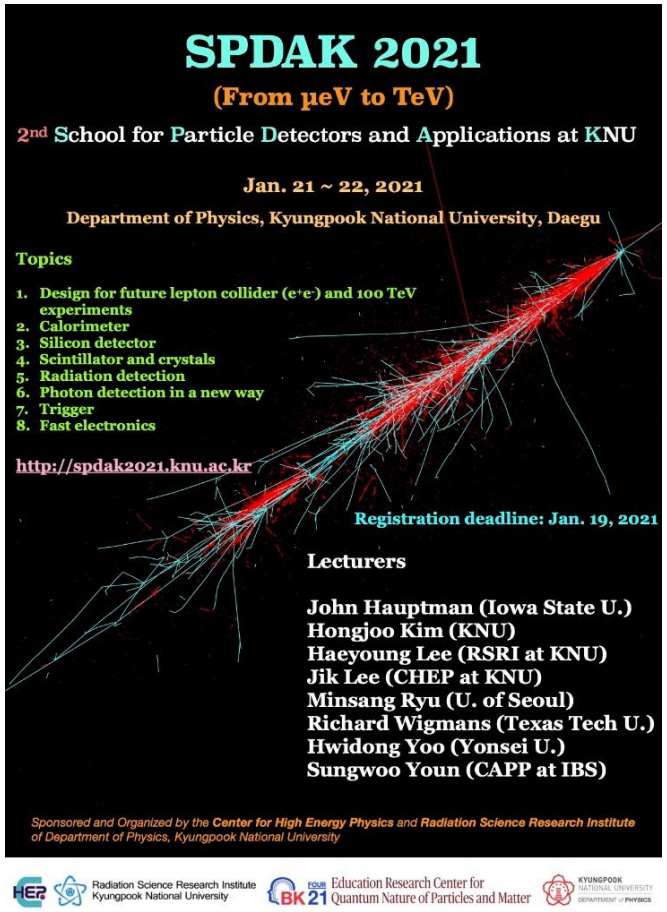
Introduction of Fast Electronics



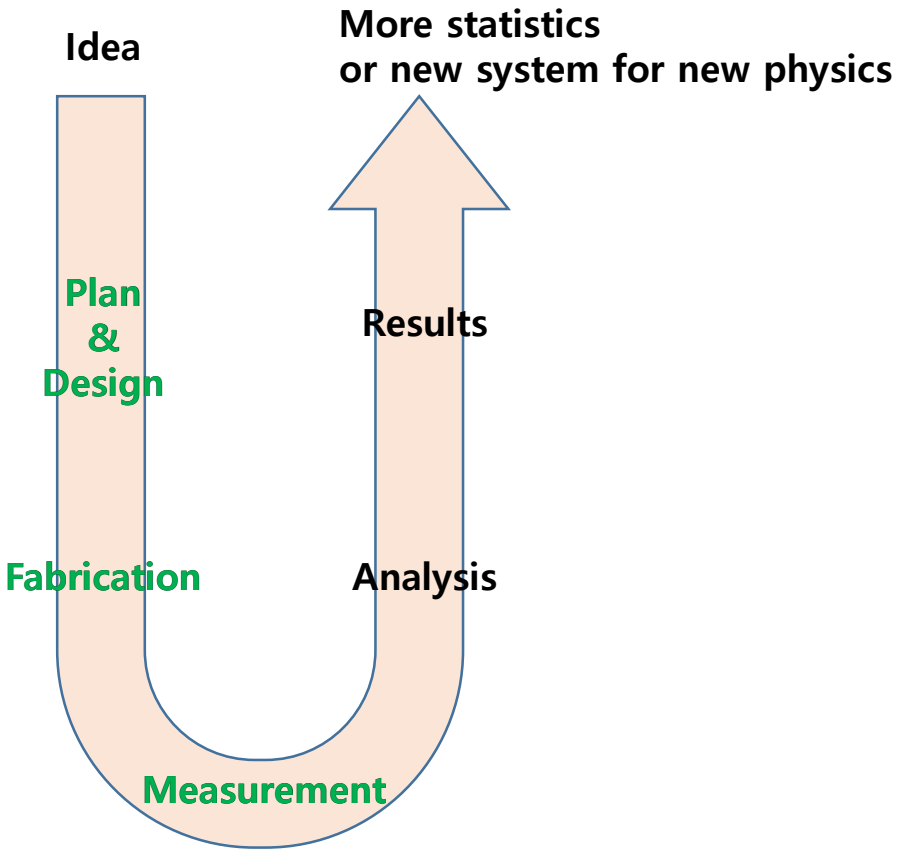
RYU, Min Sang

University of Seoul

- **Role of DAQ in HEP experiment**
- **Readout scheme for DAQ**
- **Fast electronics**
  - Signal and Device impedance
  - Preamplifier
  - Fan-In and Fan-Out
  - Discriminator (LED & CFD)
  - Logic Unit for coincidence
  - TDC & ADC
- **Summary**

Role of DAQ System in HEP experiment

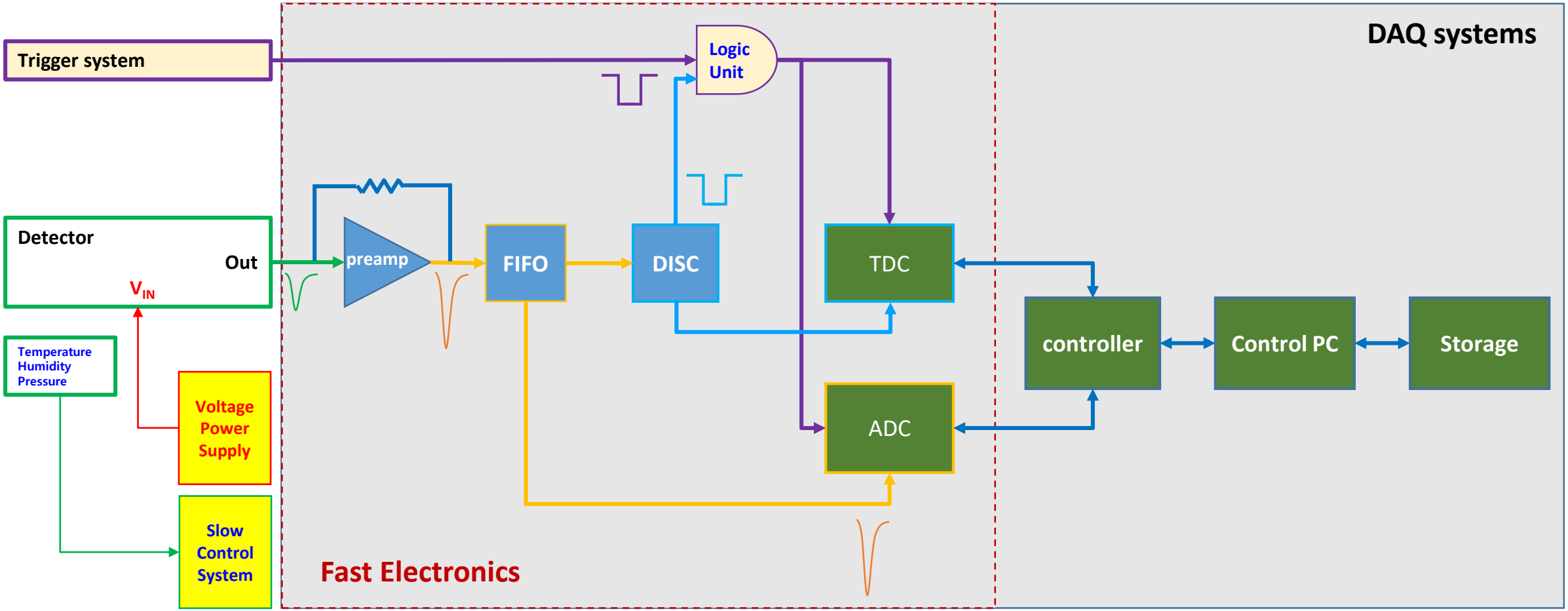
How do we watch an event in HEP experiments?



Five Ws & Hows	Measurement of particle detection
Why	Why needs information about particles ➔ to find out why they are existed and created
	Plan & Design ➔ Fabrication ➔ Measurement
How	How particle interacts with materials
Where	Position where interaction happens
When	Time when interaction happens
Who/Which	Which particles ➔ PID
What	What characteristics of particles

We design, fabricate, test, and use the readout system (or fast electronics) for data acquisition (DAQ).

Readout scheme for data acquisition (DAQ)



Components of waveform

Base line
Pulse height
Pulse width

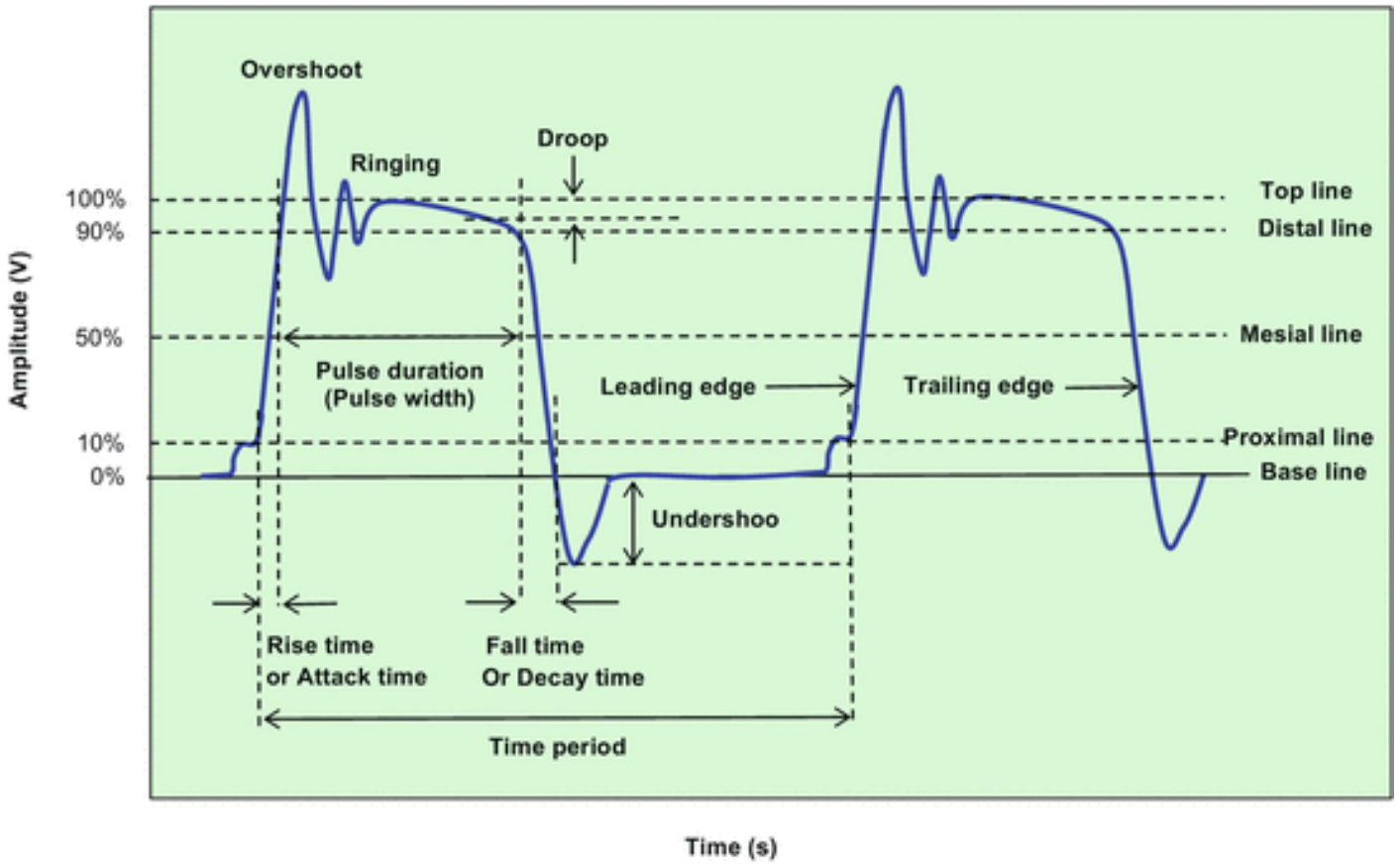
Proximal line: 10% of pulse height
Mesial line: 50% of pulse height
Distal line: 90% of pulse height

Rise time (or attack time) **at leading edge**
Fall time (or decay time) **at trailing edge**
➔ These depend on the polarity of waveform.

Overshoot
Undershoot
Ringing

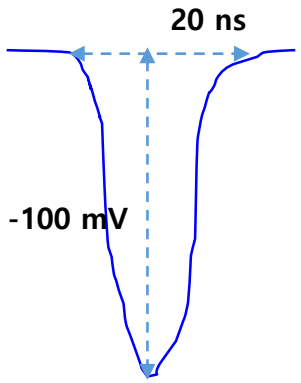
Time period

https://link.springer.com/chapter/10.1007/978-3-319-25448-7_7

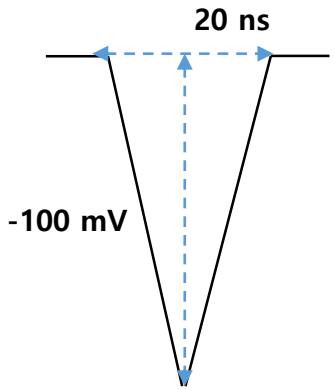


Charge of raw signal

Raw signal



Assumption



Electric charge of analog signal with assumption:

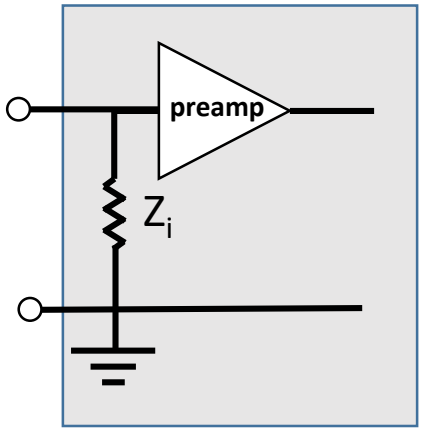
$$Q(C) = \frac{V(V) \cdot t(s)}{2 \cdot R(\Omega)} = \frac{-0.1\,V \cdot 20\,ns}{2 \cdot 50\Omega} = -20\,pC$$

Device impedances

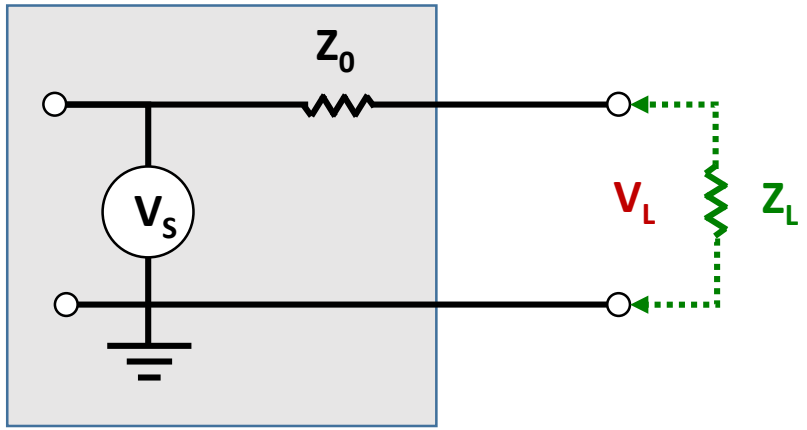
Radiation Detection and Measurement, Glenn F. Knoll

A basic concept in the processing of pulses from radiation detectors is the impedance of the devices that comprise the signal-processing chain.

Input configuration



output configuration



Voltage (V_L) appearing across a loading (Z_L) by voltage-divider relation

$$V_L = V_S \frac{Z_L}{Z_0 + Z_L}$$

For the open-circuit or unloaded ($Z_L = \infty$), voltage is $V_L = V_S$. ➔ not for the real experiment

To preserve maximum signal level, one normally wants V_L to be as large a fraction of V_S as possible.
For $Z_L \gg Z_0$ then $V_L \cong V_S$ ➔ Fan-In & Fan-Out, Discriminator, ADC, etc

For $Z_L = Z_0$ then $V_L = V_S/2$ ➔ Divider or Splitter

Preamplifier

Radiation Detection and Measurement, Glenn F. Knoll
https://www.sciencedirect.com/topics/physics-and-astronomy/preamplifiers

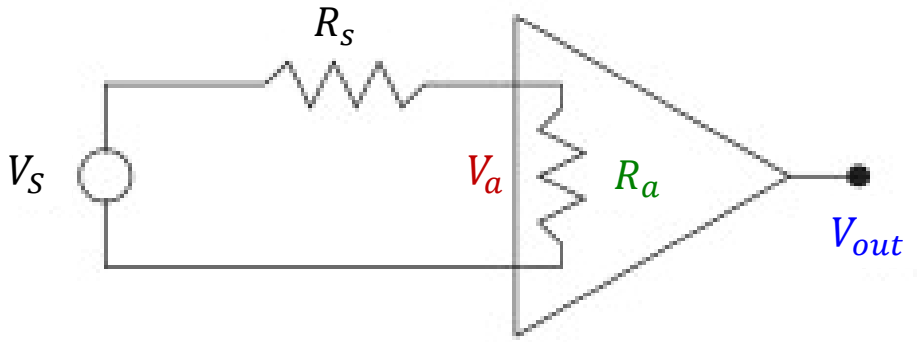
Role	**converting a raw signal from the detector into output signal with gain**
Location	**placing close to the detector to reduce the noise and avoid the signal loss**

✓ **Specification for design**
- Dynamic range
- Size of input signal
- Pulse pileup
- Signal-to-noise ratio
- Power consumption

✓ **Configuration**
- Voltage-sensitive preamplifiers
- Current-sensitive preamplifiers
- Charge-sensitive preamplifiers

Voltage-sensitive preamplifiers

https://www.sciencedirect.com/topics/physics-and-astronomy/preamplifiers



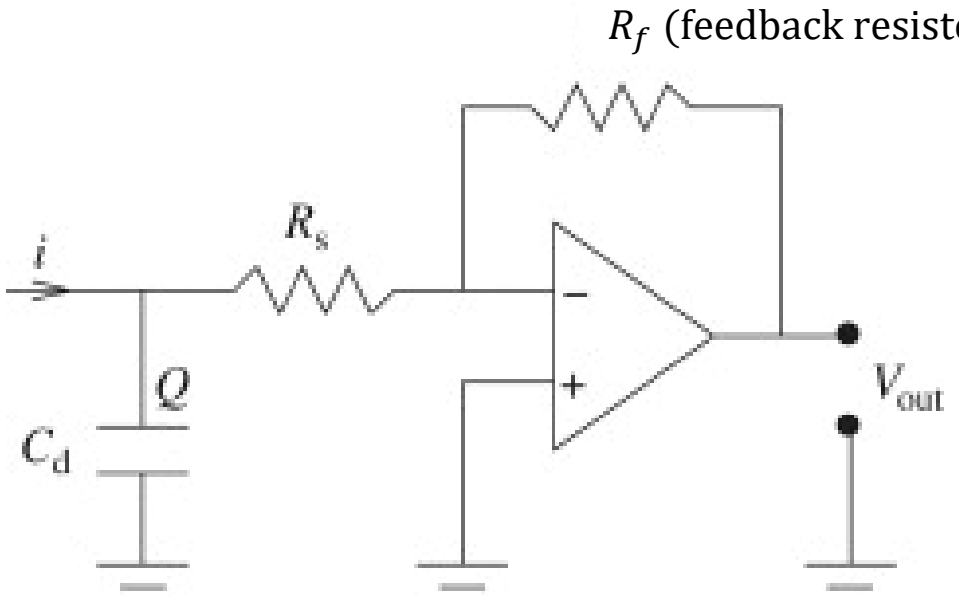
Design principle of V-sensitive preamp

Signal voltage V_S
Voltage at the input stage of the amplifier V_a
Output voltage V_{out}

$$V_a = V_S \frac{R_a}{R_s + R_a}$$

Any current drawn would decrease the potential drop across R_s.
Ideally, its input resistance have to be infinite.
But it can only be achieved up to a good approximation.

For $R_a \gg R_S$ then $V_a \cong V_S$
then $V_{out} = Gain \times V_a \approx Gain \times V_S$



Simplified realistic V-sensitive preamp

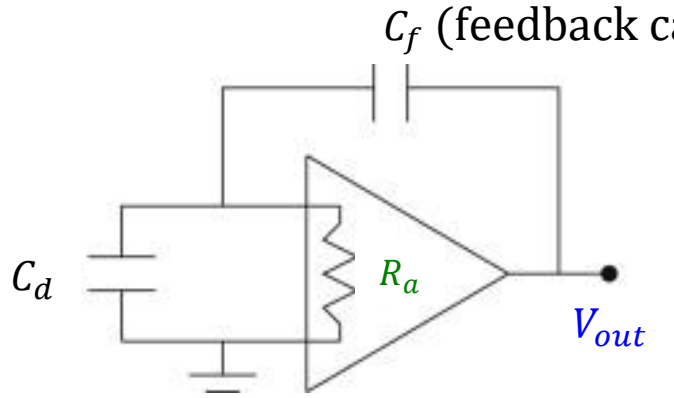
Signal voltage $V_S = Q/C_d$
Q: collected charge on the readout electrode ($Q = \int_0^{t_0} i_s(t)\,dt$)
C_d: combined detector and stray capacitance

then $V_{out} \approx Gain \times \frac{Q}{C_d} = \frac{Gain}{C_d} \int_0^{t_0} i_s(t)\,dt$

Since we are integrating the current to convert it into voltage, **C_d should discharge slower than the charge collection time** $t_d << R_aC_d$.

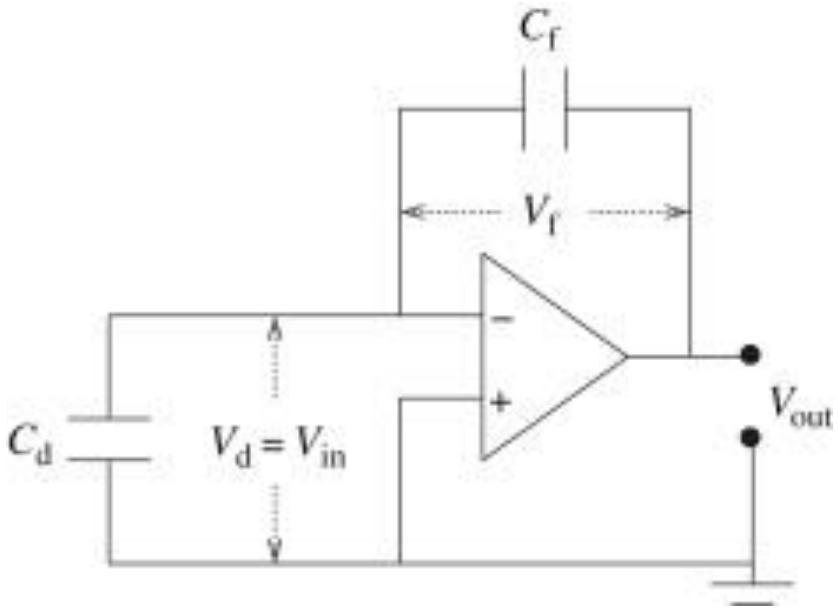
Charge-sensitive preamplifiers

https://www.sciencedirect.com/topics/physics-and-astronomy/preamplifiers



Basic principle of Q-sensitive preamp

The dependence of a voltage-sensitive preamplifier on the input capacitance is a serious problem for many detection systems.
➔ to develop Q-sensitive preamplifiers



Simple Q-sensitive preamp

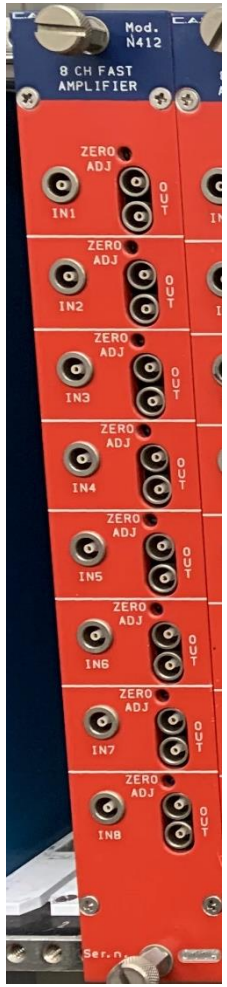
The charge (Q_d) accumulated on the electrode (C_d) is integrated on another capacitor (C_f). Then the potential (V_f) on that capacitor is then directly proportional to the original charge (Q_d) on the detector.

$$V_{out} \propto \frac{Q_f}{C_f} \propto \frac{Q_d}{C_f}$$

The condition that $Q_f \approx Q_d$ can only be achieved if no current flows into the preamplifier's input with $R_a \rightarrow \infty$.

Preamplifiers

https://www.caen.it



CAEN N412 8ch Fast Amplifier

INPUTS:

- 50Ω impedance.
- Reflection coefficient: ≤ 6% over input dynamic range.
- Quiescent voltage: < ± 5 mV.

OUTPUTS:

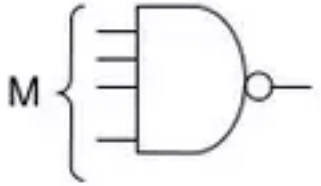
- Risetime: ≤ 3.0 ns.
- Falltime: ≤ 2.0 ns.
- Maximum positive amplitude (linear): 400 mV (50Ω impedance).
- Maximum negative amplitude (linear): -4 V (50Ω impedance).
- Overshoot: ± 10% for input risetimes of 2 ns and with the 2nd output terminated in 50Ω.
- Quiescent voltage adjustable (via front panel trimmer for each channel) in the range from -20 mV to +50 mV.

GENERAL:

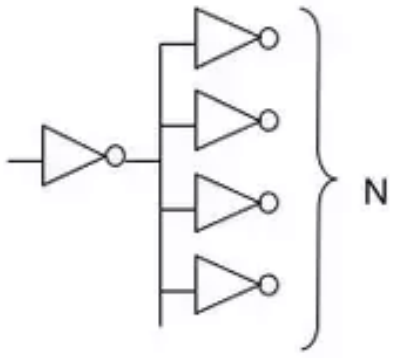
- Gain: fixed 10 ± 3%, non-inverting.
- Coupling: direct.
- I/O delay: ≤ 12 ns.
- Noise: less than 1 mV, referred to input.
- Interchannel crosstalk: better than -56 dB in the worst test condition, and with both the outputs of the tested channel terminated in 50Ω.
- Bandwidth:
  - 160 MHz (with both the channel's outputs terminated in 50Ω);
  - 180 MHz (single ended output).

Fan-In and Fan-Out (FIFO)

Fan-in: maximum number of input signals feeding into the input of a logic system

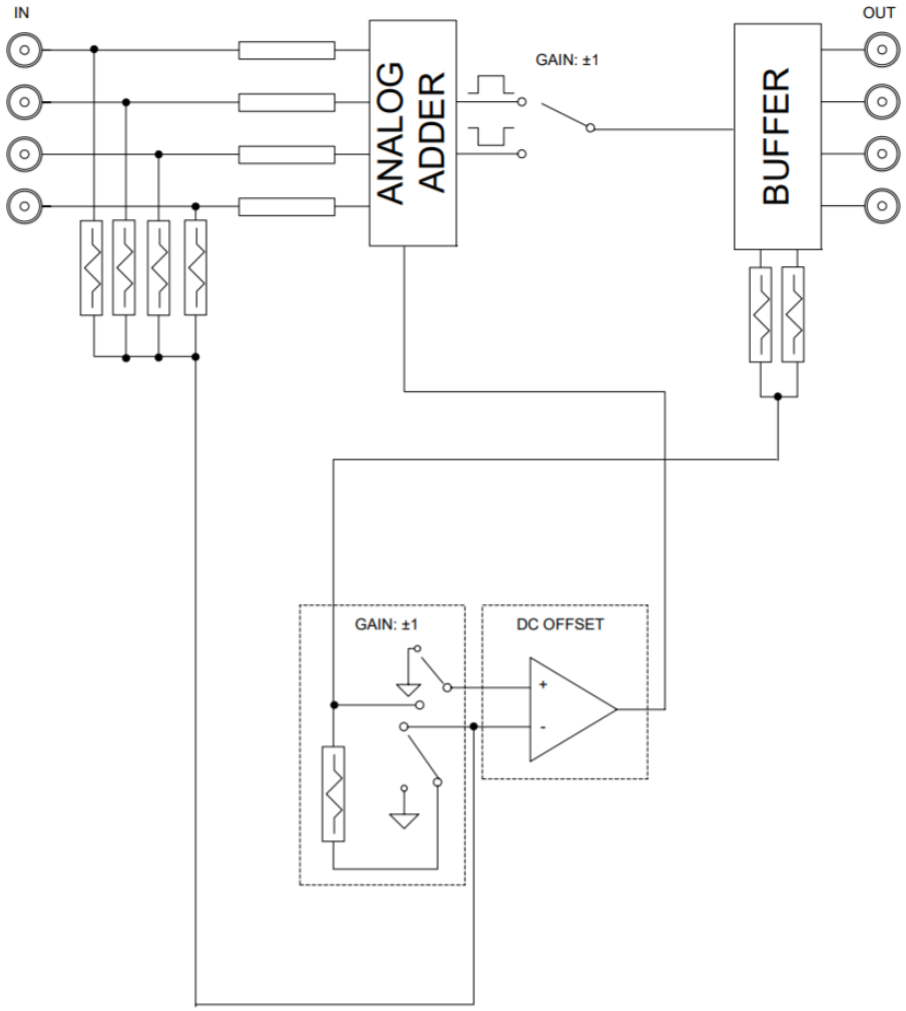


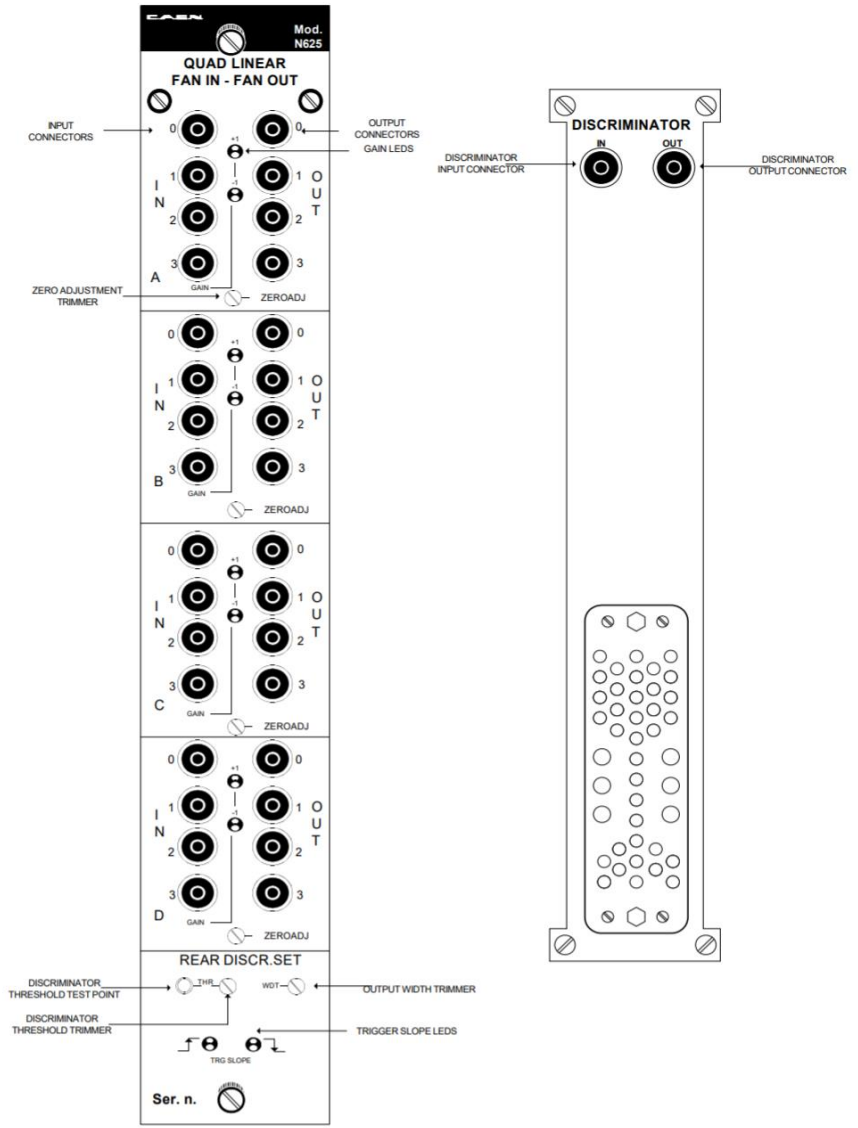
Fan-out: maximum number of output signals from the output of a logic system



Fan-In and Fan-Out (FIFO)

https://www.caen.it





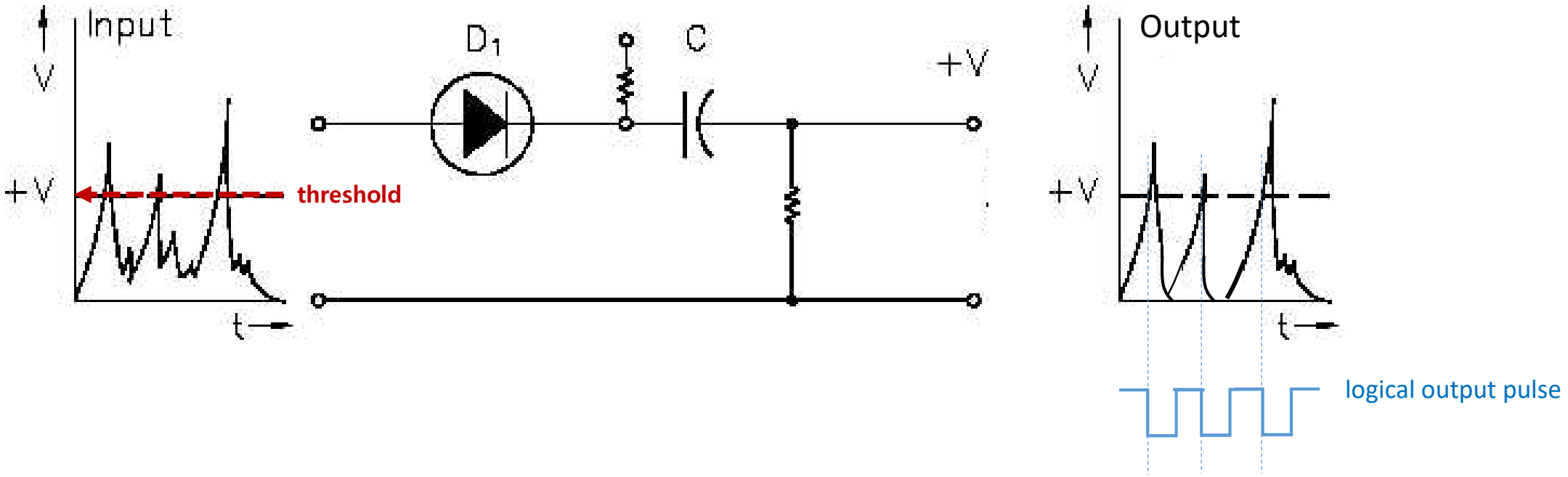
CAEN N625 Quad Linear Fan In / Fan Out

Discriminator (DISC)

http://nuclearpowertraining.tpub.com/h1013v2/css/Discriminator-Circuit-83.htm

Role: generating the logical output pulse when the input pulse exceeds the discriminator preset level

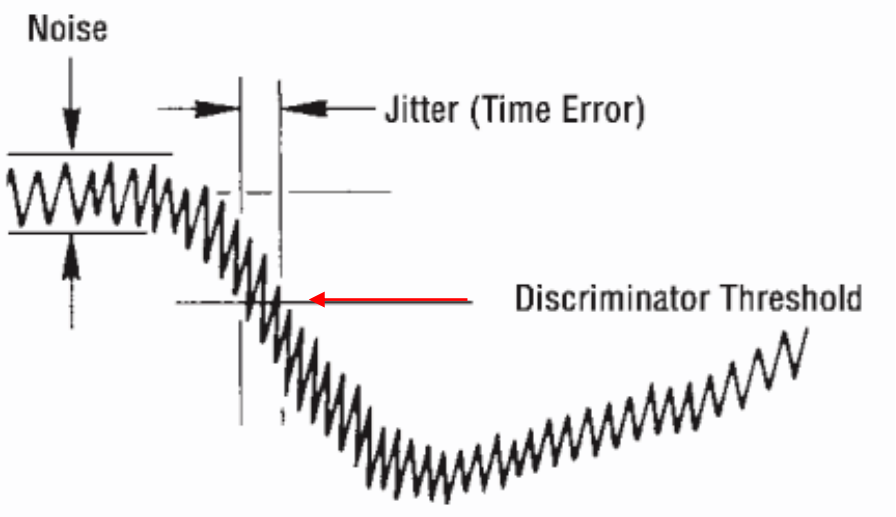
➔ If input voltages **exceeds the threshold value +V** then diode D_1 conducts and **DISC generates the logical output pulses**.



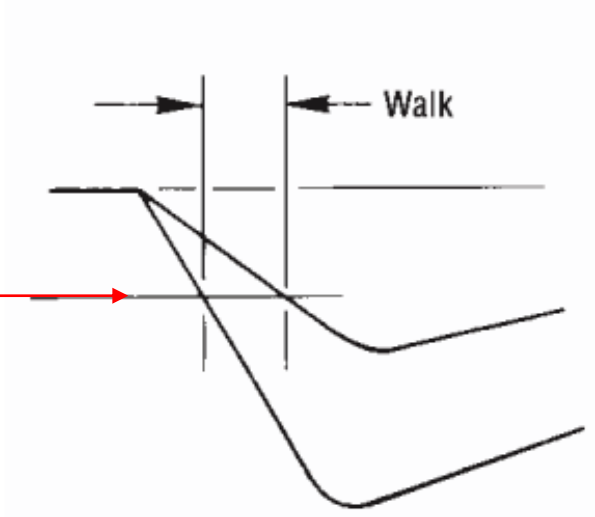
Timing jitter and walk

http://www.peo-radiation-technology.com/wp-content/uploads/2015/09/ort_15_fast-timing-discriminators_datasheet_peo.pdf

Timing jitter in a pulse



Timing walk among pulses



The contribution of noise to the (Timing) Jitter

$$\textbf{Timing Jitter} = e_{noise}/(dV/dt)$$

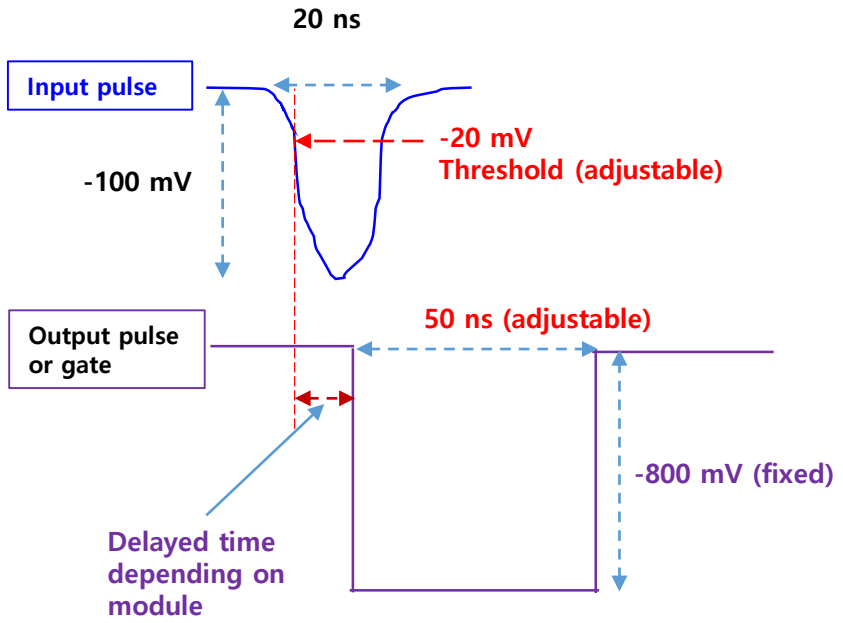
e_{noise}: voltage amplitude of the noise superimposed on the analog pulse

dV/dt: slope of the signal when its leading edge crosses the discriminator threshold

"(Timing) Walk" is the **systematic dependence** of the time marker **on the amplitude of the input pulse.**

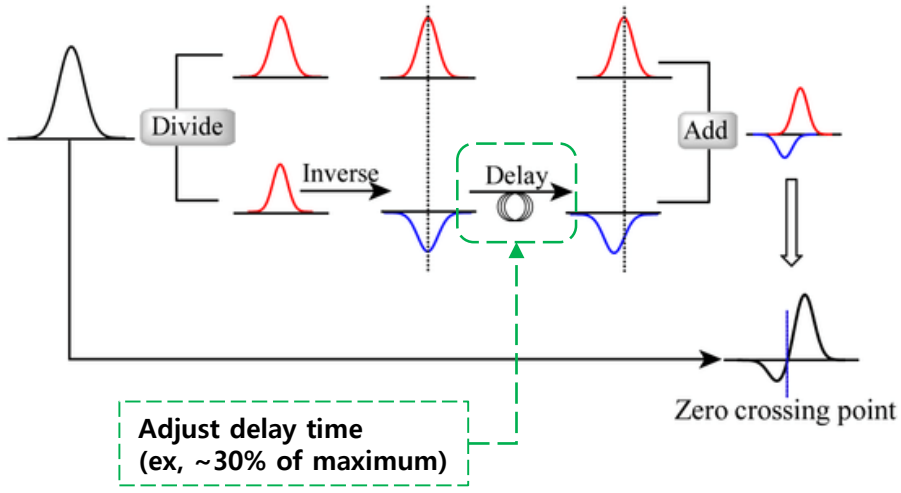
LED and CFD

Leading Edge Discrimination (LED)



Constant Fraction Discrimination (CFD)

Tuhin Khan's Ph. D. thesis



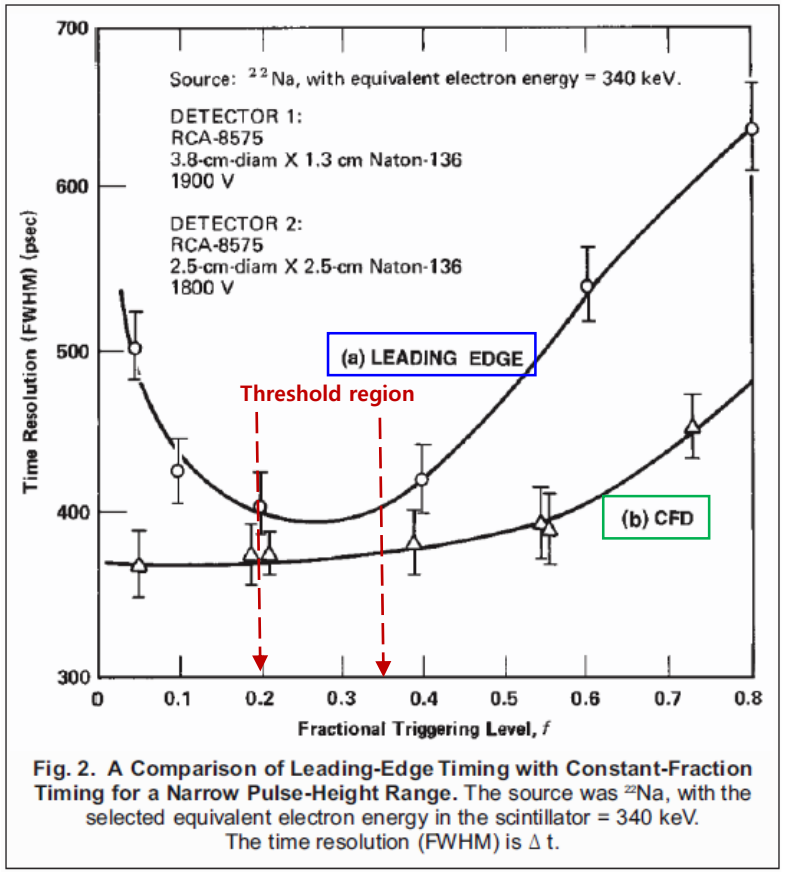


Fig. 2. A Comparison of Leading-Edge Timing with Constant-Fraction Timing for a Narrow Pulse-Height Range. The source was ^{22}Na, with the selected equivalent electron energy in the scintillator = 340 keV. The time resolution (FWHM) is Δ t.

http://www.peo-radiation-technology.com/wp-content/uploads/2015/09/ort_15_fast-timing-discriminators_datasheet_peo.pdf

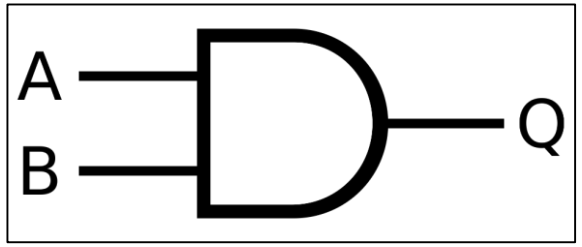
Time resolution: $\sigma_{CFD} < \sigma_{LED}$

Role of Logic Unit

https://www.wekipedia.com

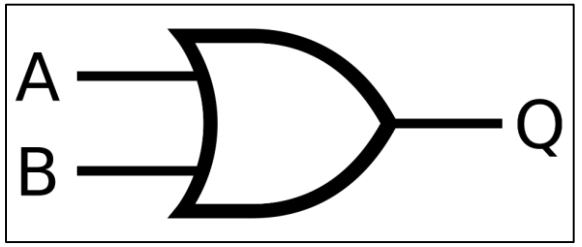
Role: generating the gating pulse when the preset of logical algorism against with inputs is true

AND logic: $A \cdot B$ or $A \wedge B$



INPUT		OUTPUT
A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1

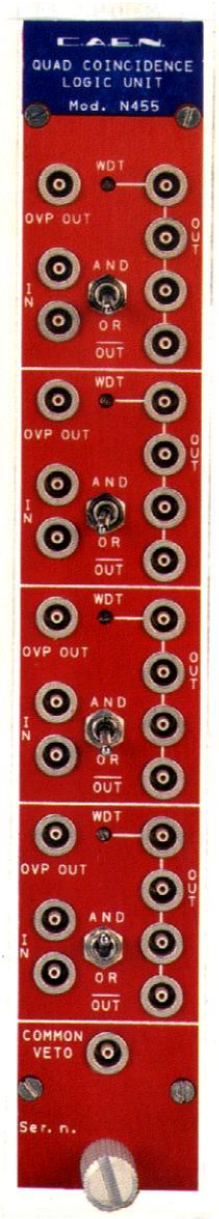
OR logic: $A + B$ or $A \vee B$

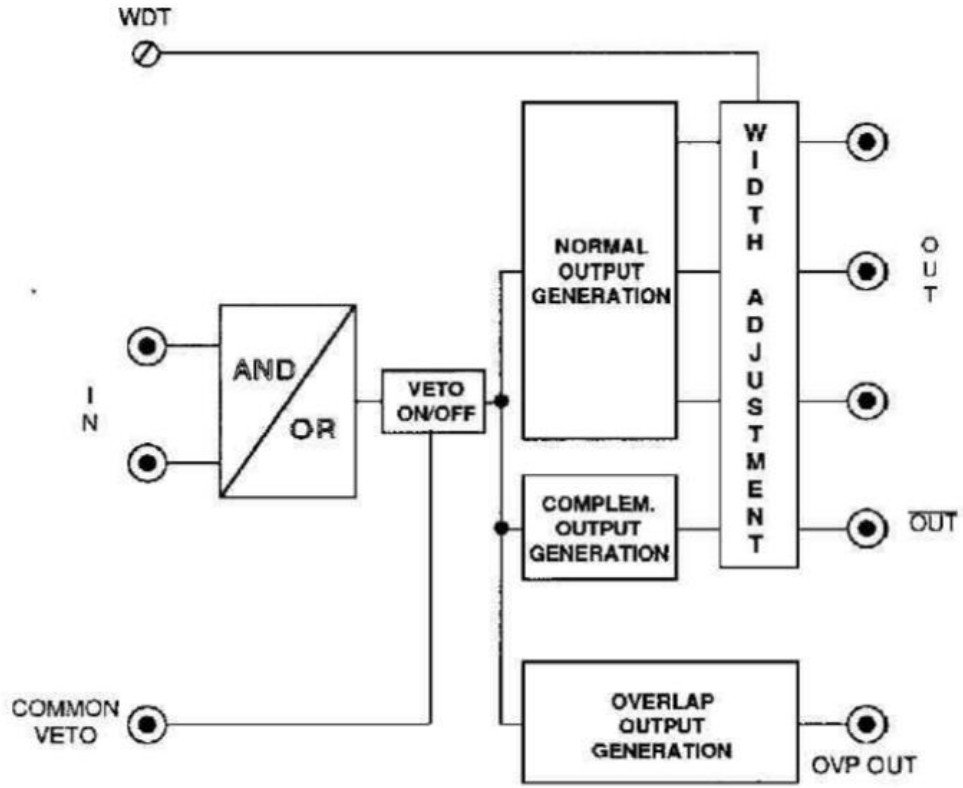


INPUT		OUTPUT
A	B	Q
0	0	0
0	1	1
1	0	1
1	1	1

Logic Unit

https://www.caen.it





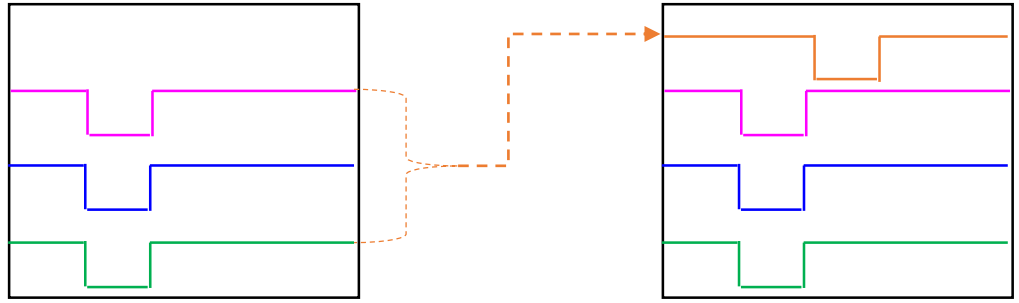
IMPORTANT NOTE:
Unused Outputs require a 50 Ω termination

CAEN N455 Quad Coincidence Logic Unit

Coincidence with 3 inputs

When events occur, **the input signals** from many detectors can be matched with Logic Unit.

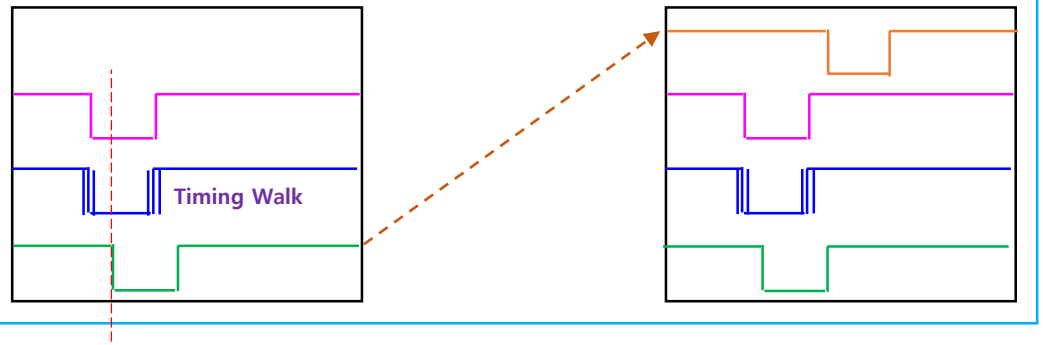
3 coincidence



Coincidence with timing walk

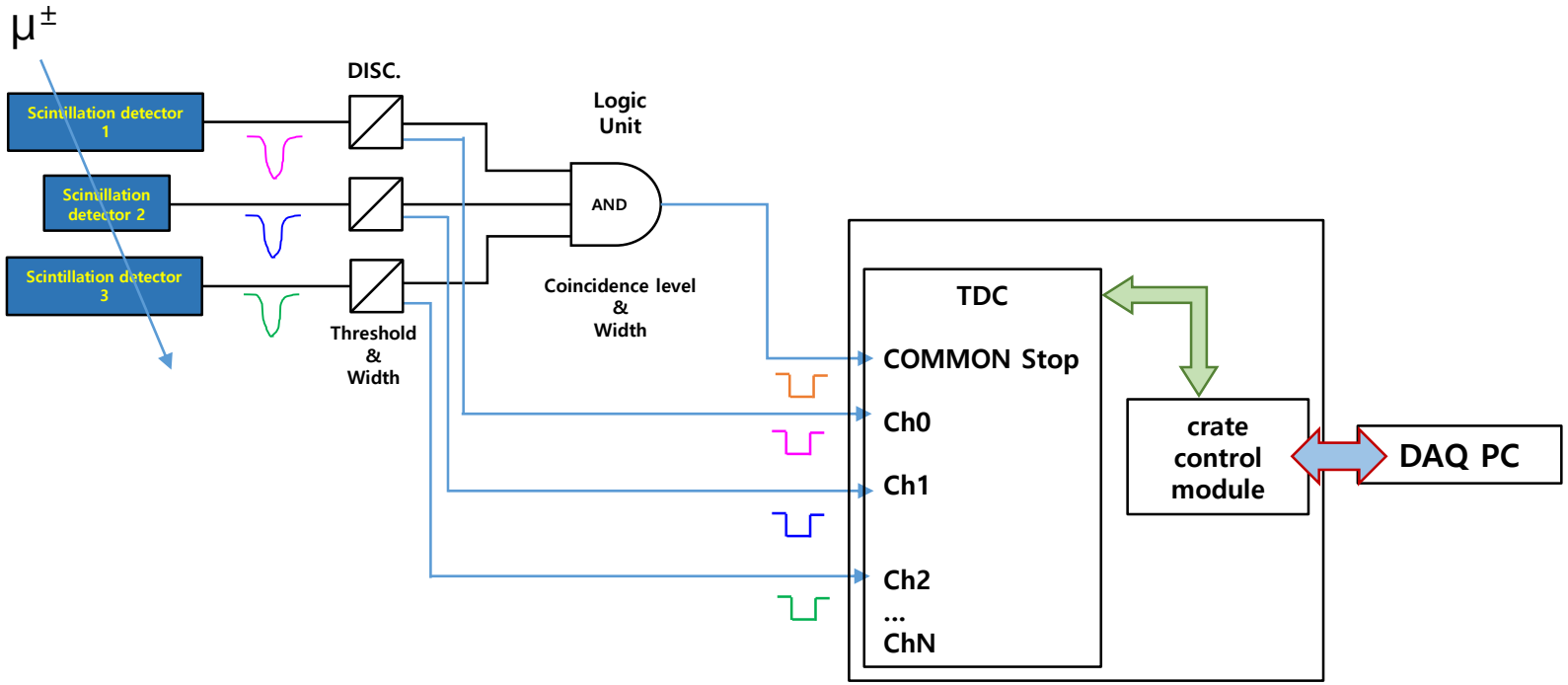
Gate (Ch2) is shaking in time domain, called ***Timing Walk***.

Gate (Ch3) delayed

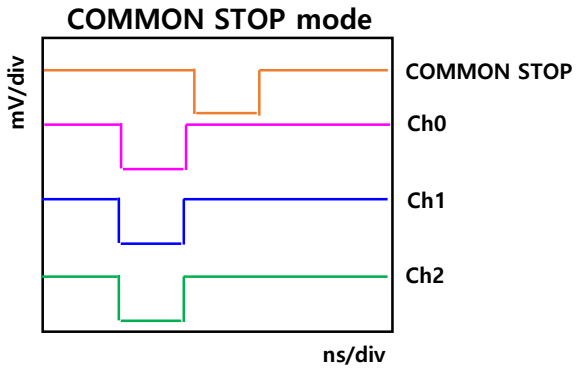


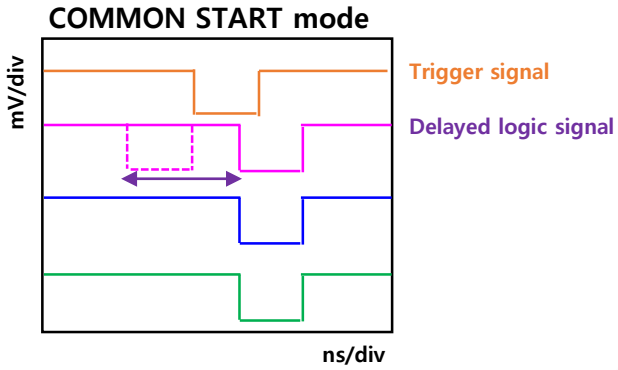
Time measurements with TDC

Scintillation counter/detector:
Scintillator + **P**hoto**M**ultiplier **T**ube (PMT)



Operation mode of TDC: COMMON STOP/START?

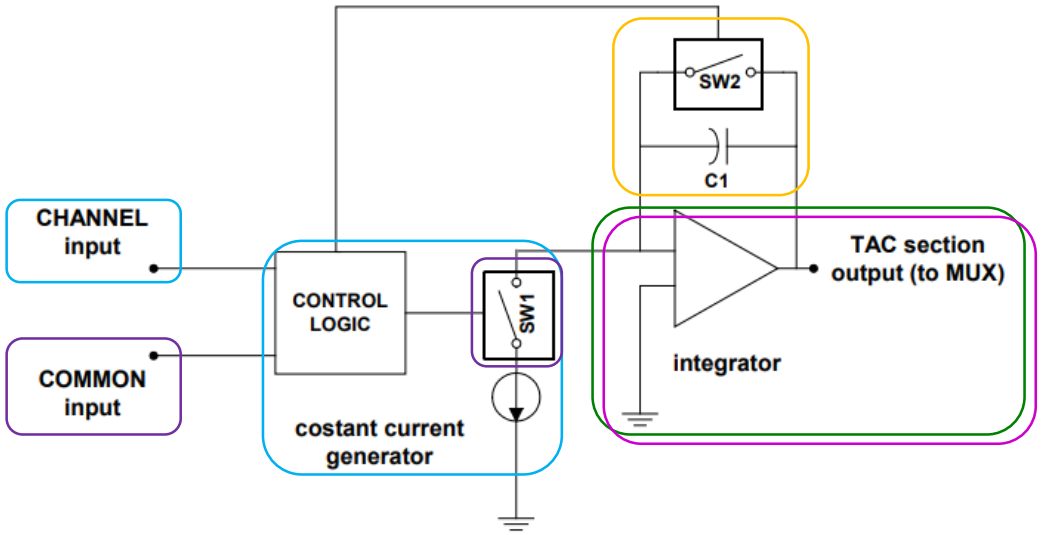




Time-to-Digital Converter (TDC)

How to record time in TDC?

https://www.caen.it



Block diagram of TAC section in CAEN V775N 16ch MultiEvent TDCs

A Start signal closes the **switch SW1** thus allowing a constant current to flow through an integrator; a Stop signal opens the **switch SW1** again.

The constant current generates a **linear ramp voltage** **which is stopped at an amplitude proportional to the time interval** between Start and Stop pulses.

After digitization the **SW2 switch** is closed by the CLEAR signal which allows the discharge of the **capacitor C1**.

Both the COMMON and CLEAR signals are controlled by the CONTROL LOGIC section.

TDC and signal conversion timing

https://www.caen.it

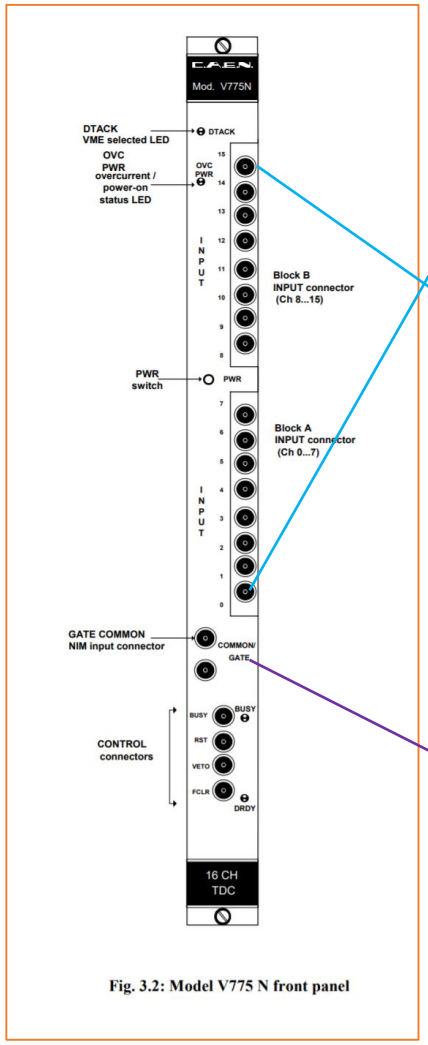
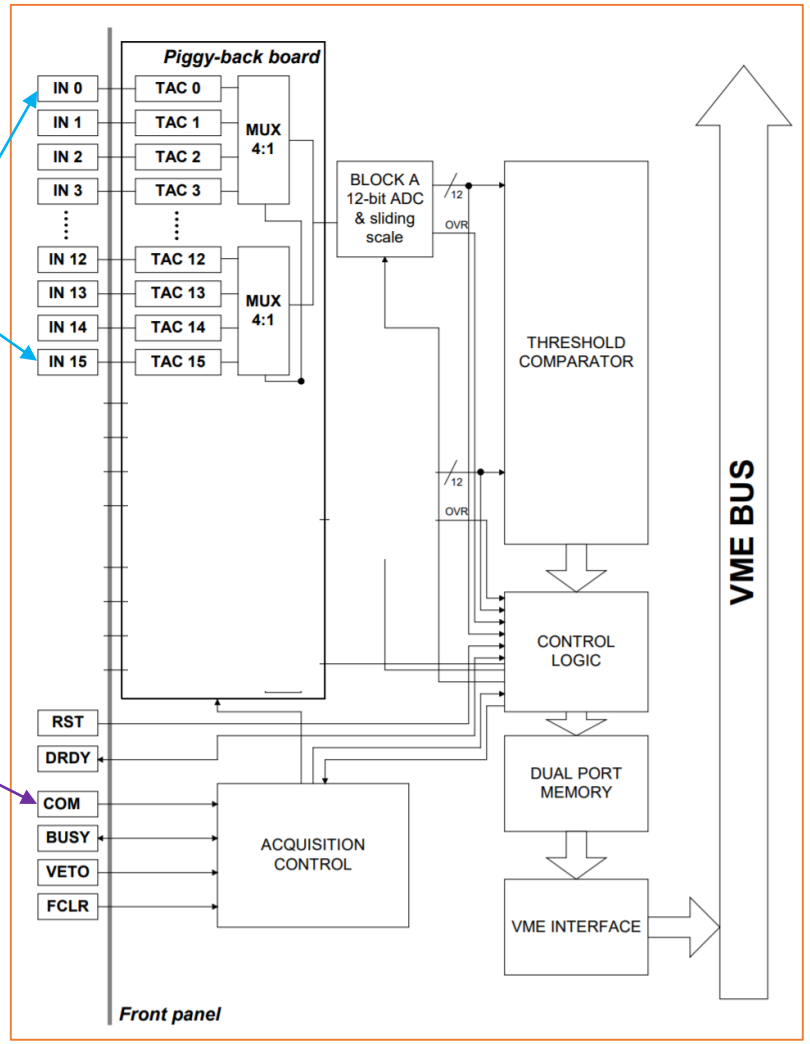


Fig. 3.2: Model V775 N front panel



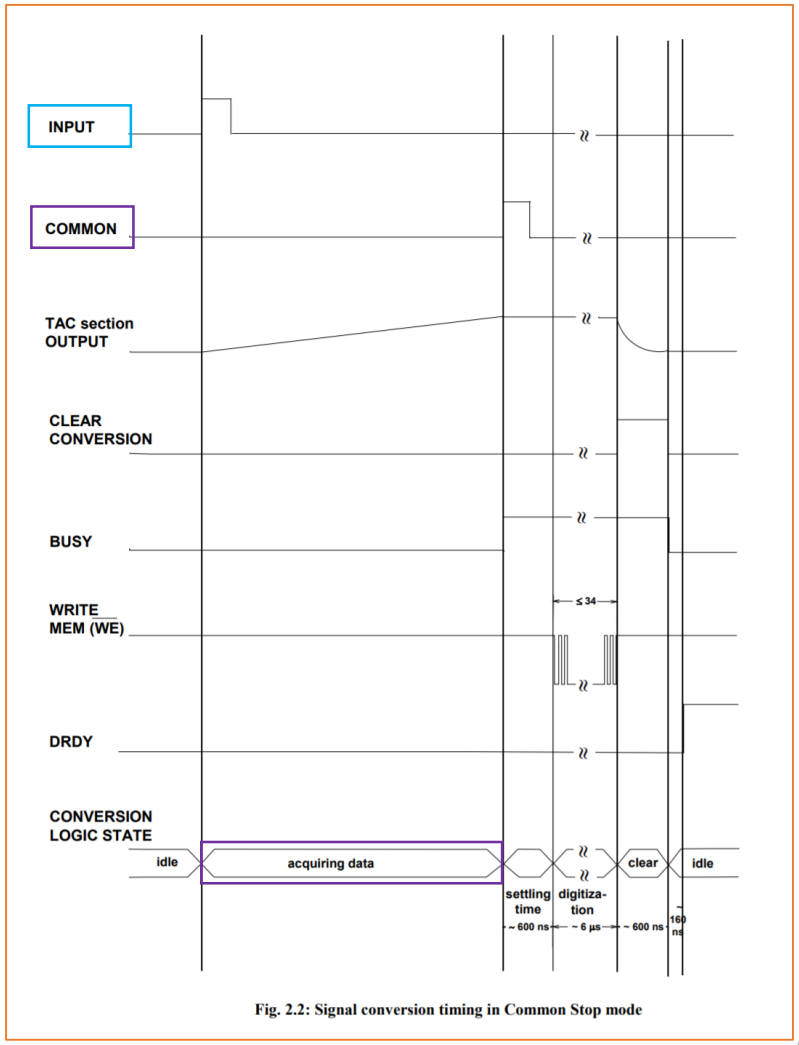
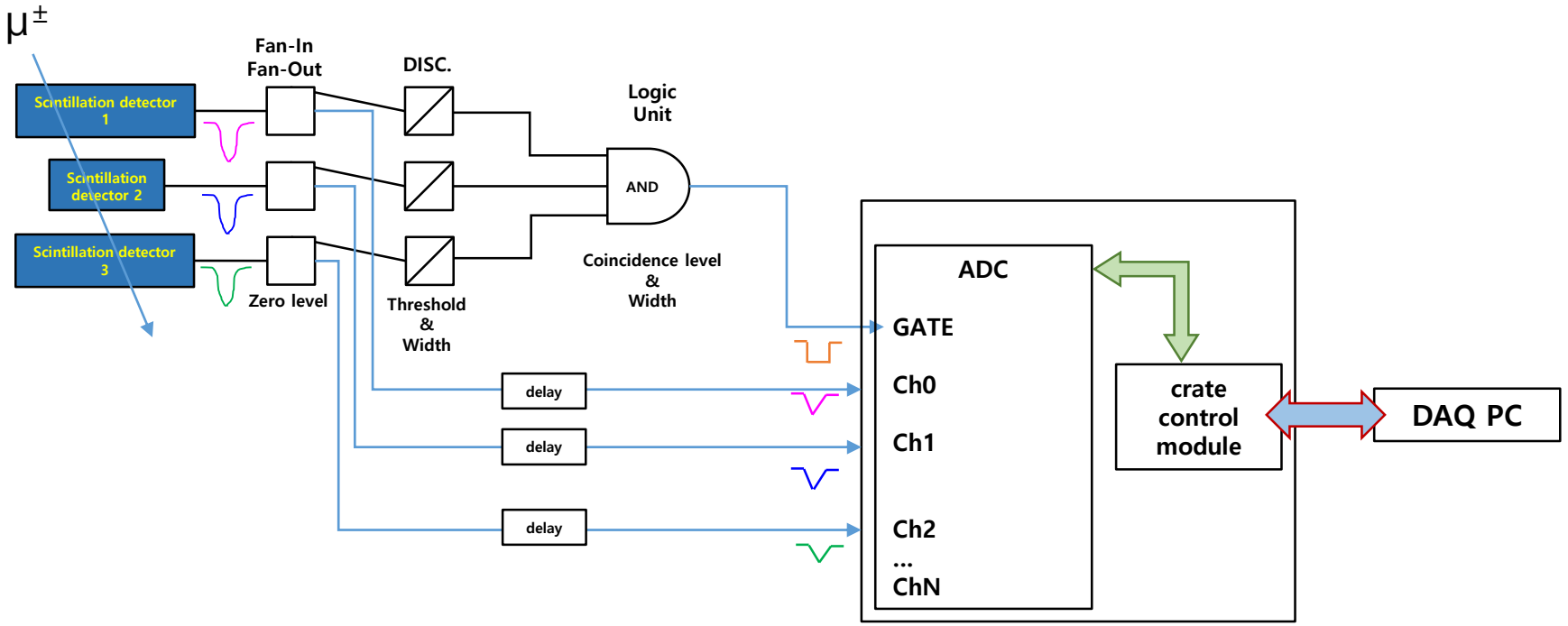


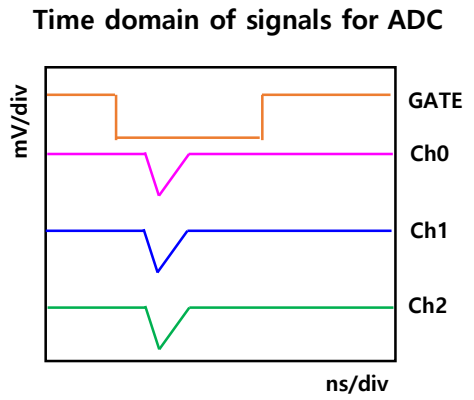
Fig. 2.2: Signal conversion timing in Common Stop mode

CAEN V775N 16ch MultiEvent TDCs

Charge measurements with ADC

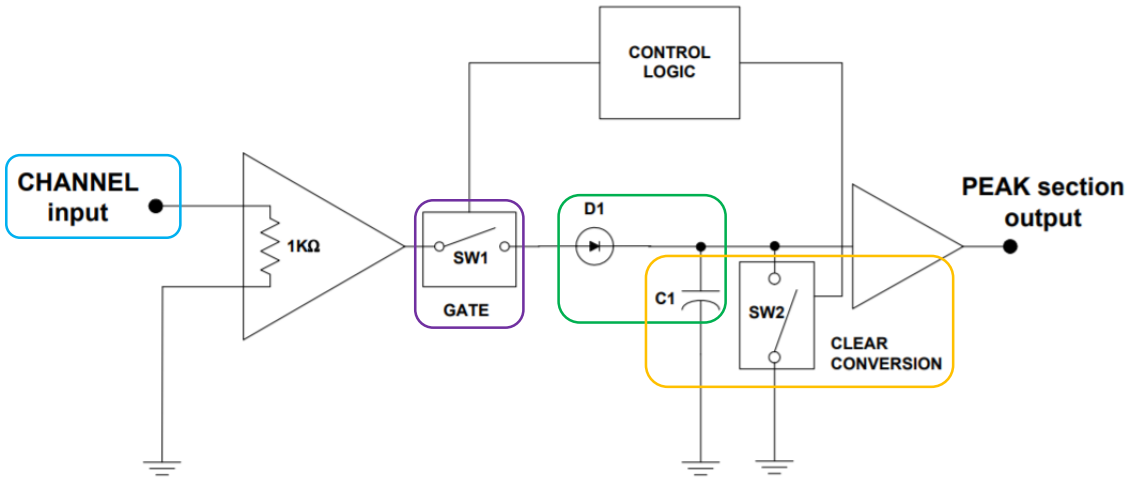
Scintillation counter/detector:
Scintillator + **P**hoto**M**ultiplier **T**ube (PMT)





How to record charge in ADC?

https://www.caen.it



Block diagram of PEAK section in CAEN V1785 8ch Dual Range Peak ADC

COMMON STOP mode

The **GATE signal** closes the **switch SW1** thus allowing the **capacitor C1** to be charged as the **diode D1** is forward-biased by the signal.

As the **SW1** is open again, the signal is digitized by the 12-bit ADCs.

After digitization the **SW2 switch** is closed by the CLEAR signal which allows the discharge of the **capacitor C1**.

Both the GATE and CLEAR signals are controlled by the CONTROL LOGIC section.

ADC and signal conversion timing

https://www.caen.it

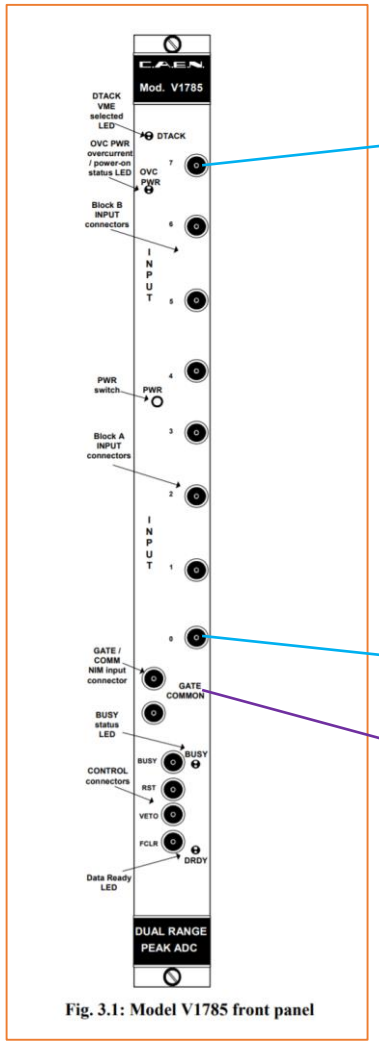


Fig. 3.1: Model V1785 front panel

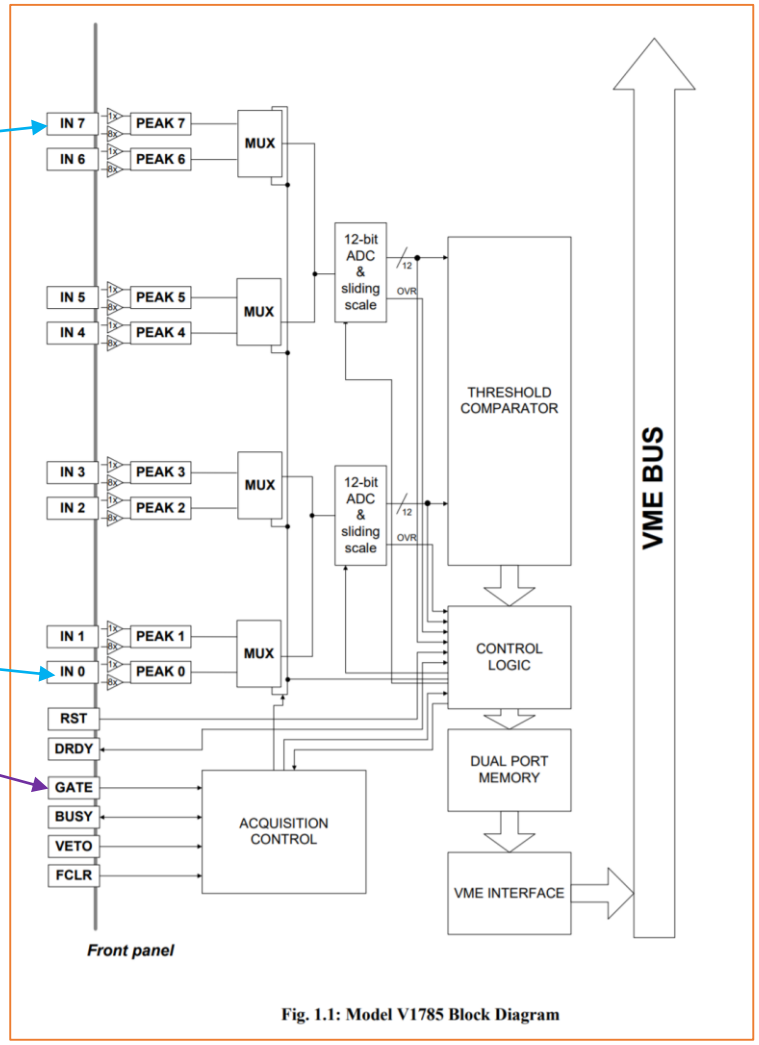


Fig. 1.1: Model V1785 Block Diagram

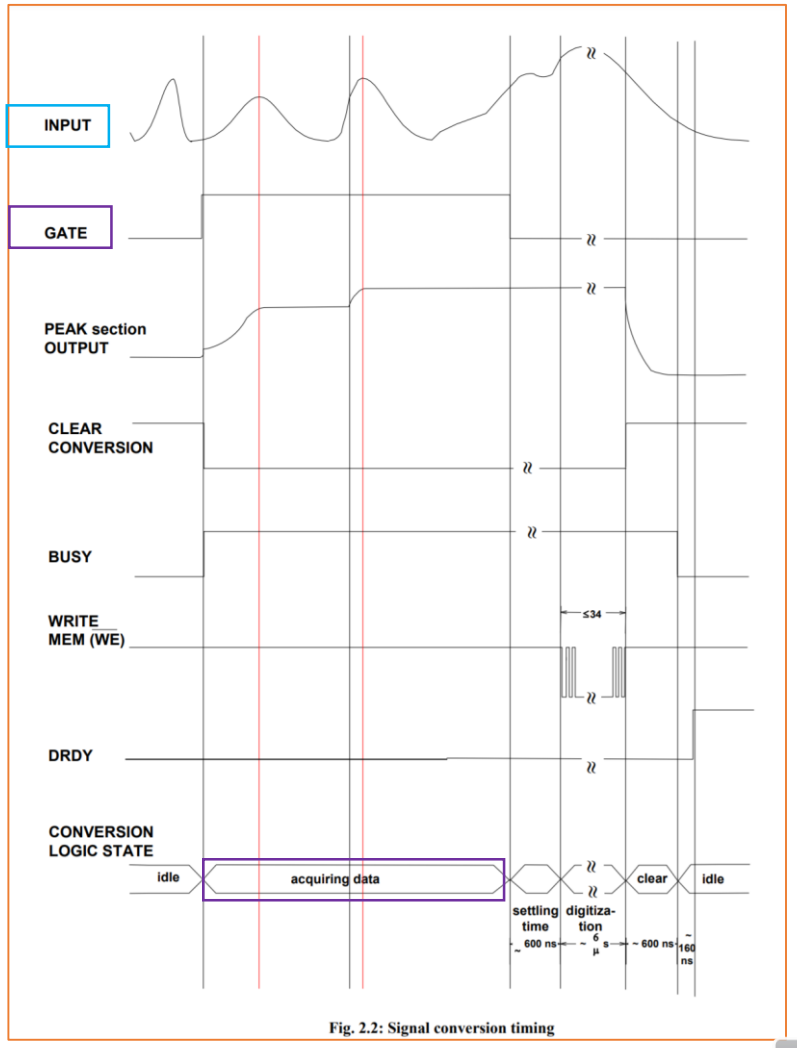


Fig. 2.2: Signal conversion timing

CAEN V1785 8ch Dual Range Peak ADC

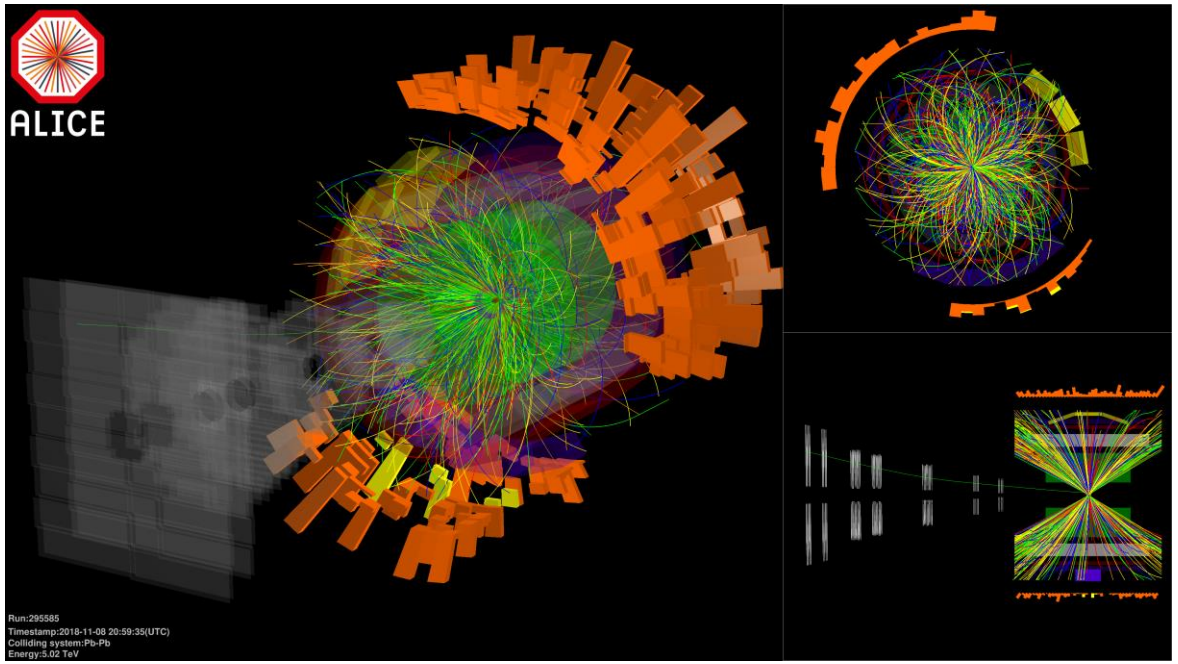
Dual input range: 0 ÷ 4 V / 0 ÷ 500 mV
Gain: 1 mV/count and 125 uV/count for High and Low ranges

Summary: Event in HEP experiment

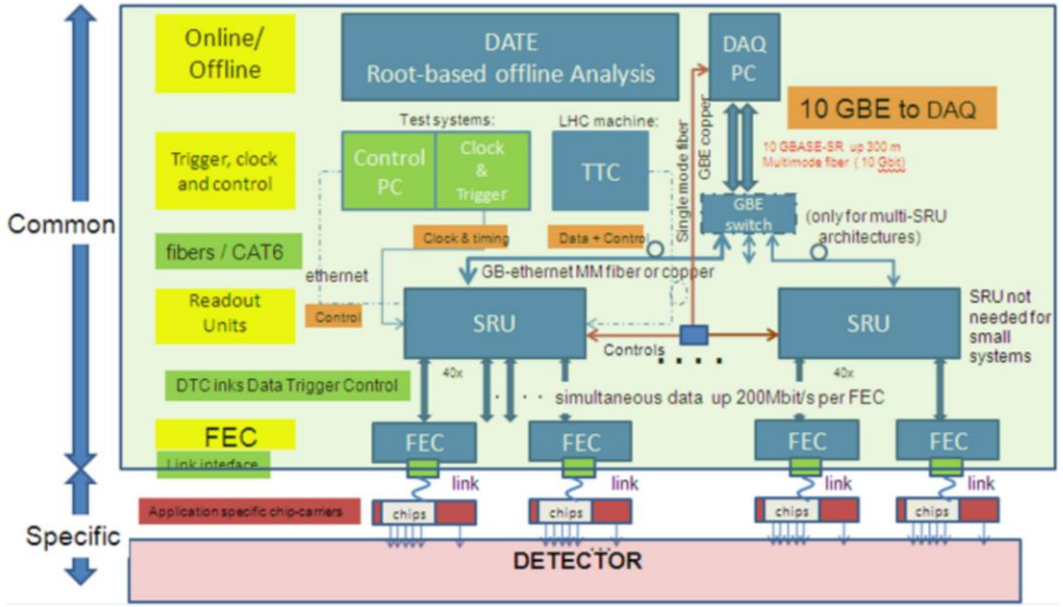
"**Fast Electronics**" are a main component of particle detection system to see what happens in the HEP experiments.

First Pb collision of ALICE experiment at $\sqrt{s}$ = 5.02 TeV in 2018

https://cds.cern.ch/record/2646381

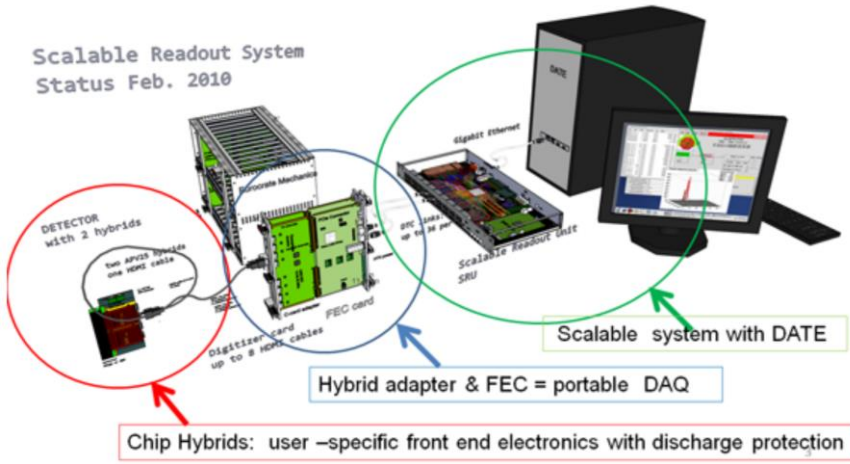


RD51 Scalable Readout System (SRS)



https://indico.cern.ch/event/77597/contributions/2088463/attachments/1056845/1506857/RD51-SRS-Description.pdf

physical overview SRS of RD51



Thank you