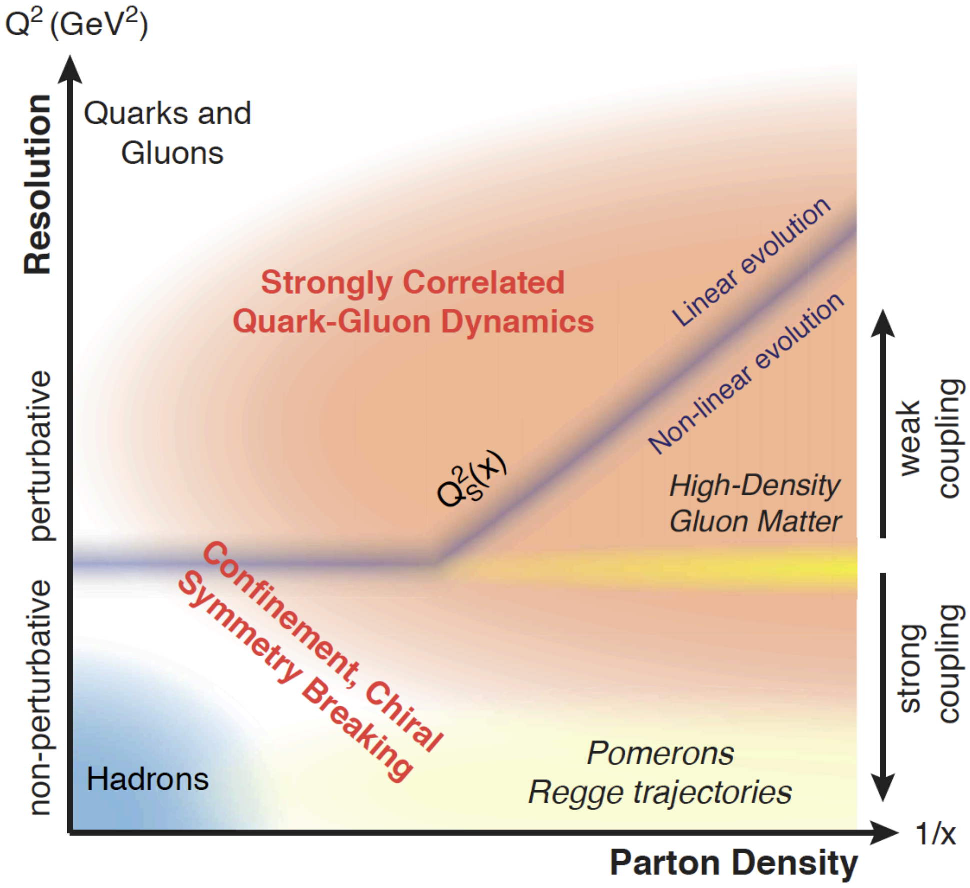
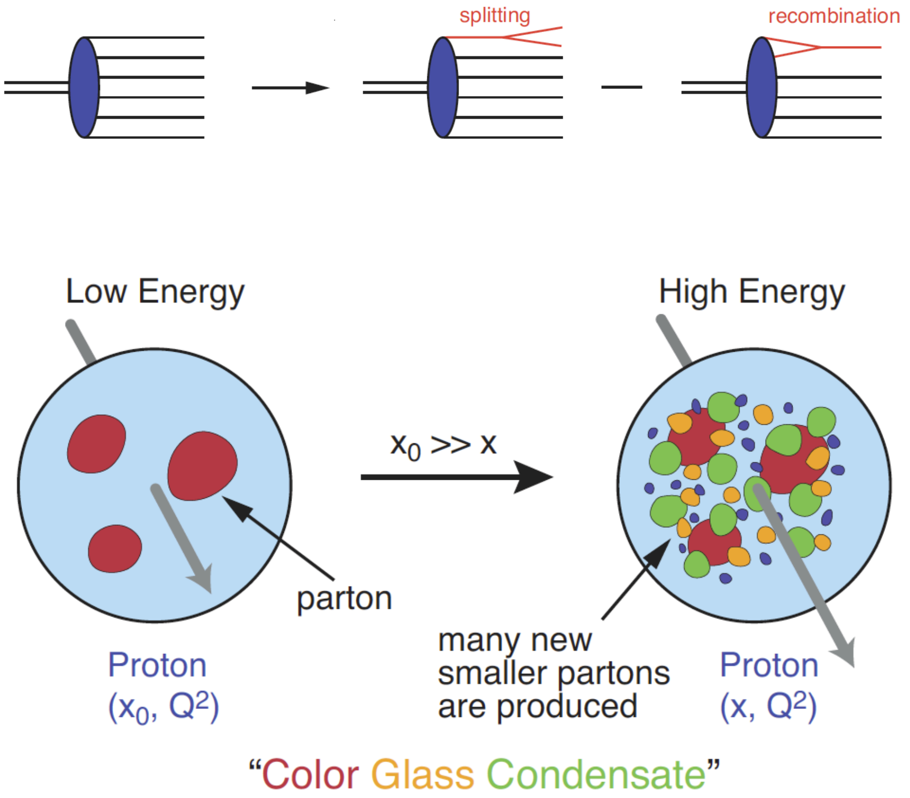
Discussion for EIC EOI
Development of silicon trackers for EIC

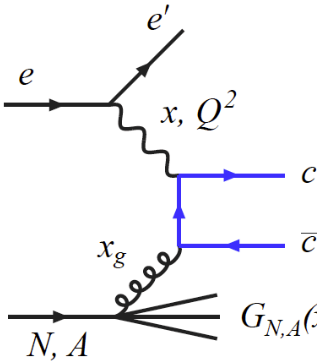
Sanghoon Lim
Pusan National University

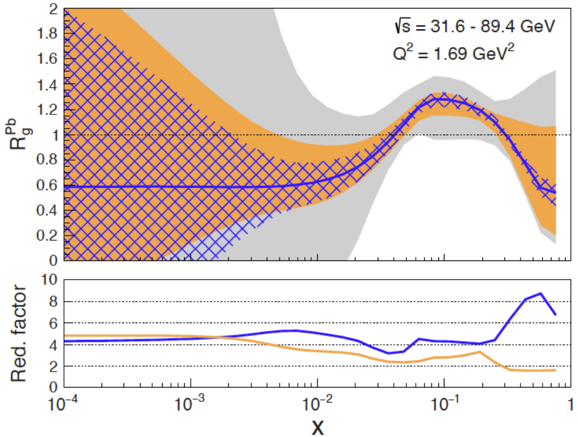
Study of gluons at the Electron Ion Collider



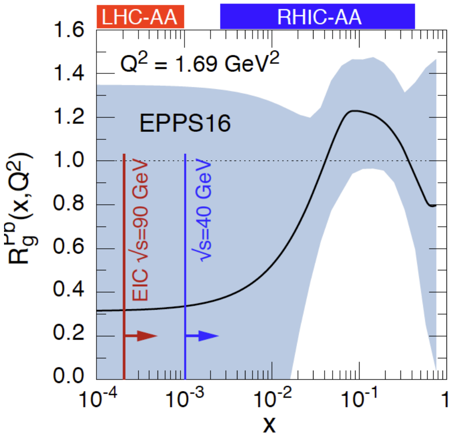


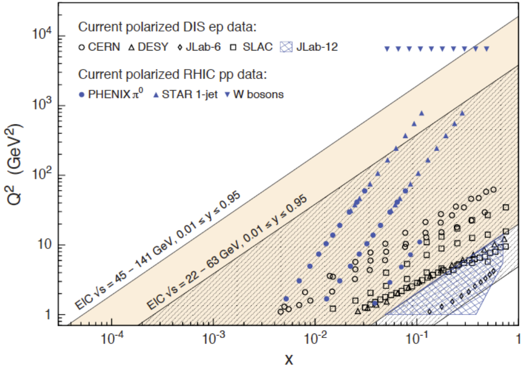
Study of gluons at the Electron Ion Collider

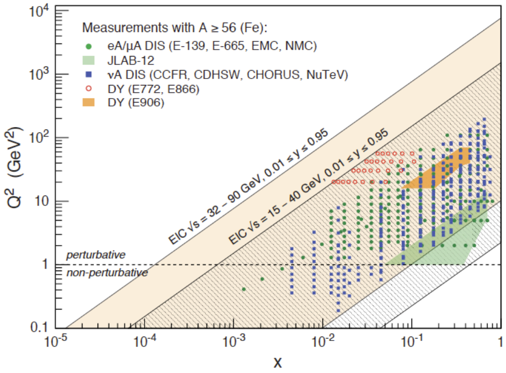




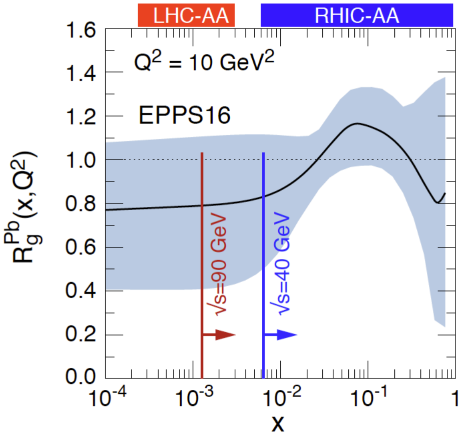
charm production from photon−glu







kinematic range in e+p and e+A



nPDF from EPPS16 and kinematic limits at EIC

2020 EIC Users Group Meeting (Jul 15-17)

Silicon Vertex Tracker at EIC (Sep 2-4)

2020 EIC Users Group Meeting

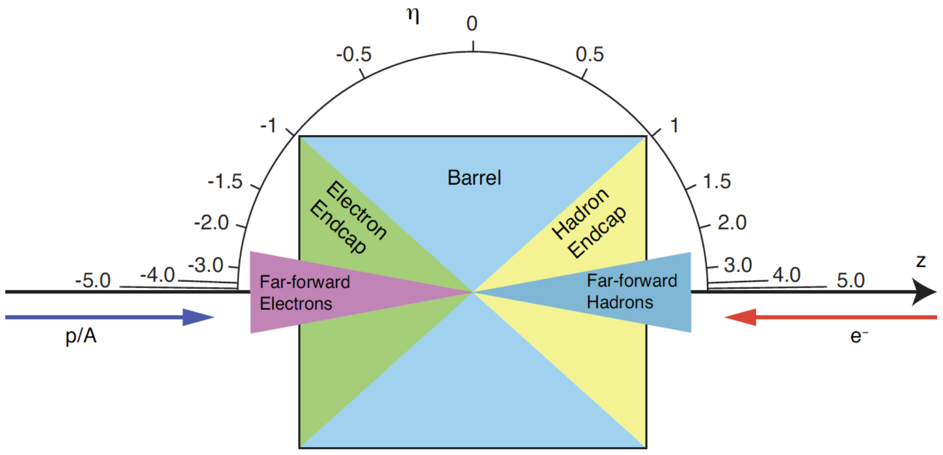
15-17 July 2020
FIU
US/Eastern timezone

SILICON PIXEL-BASED PARTICLE VERTEX AND TRACKING DETECTORS TOWARDS THE US ELECTRON ION COLLIDER WORKSHOP

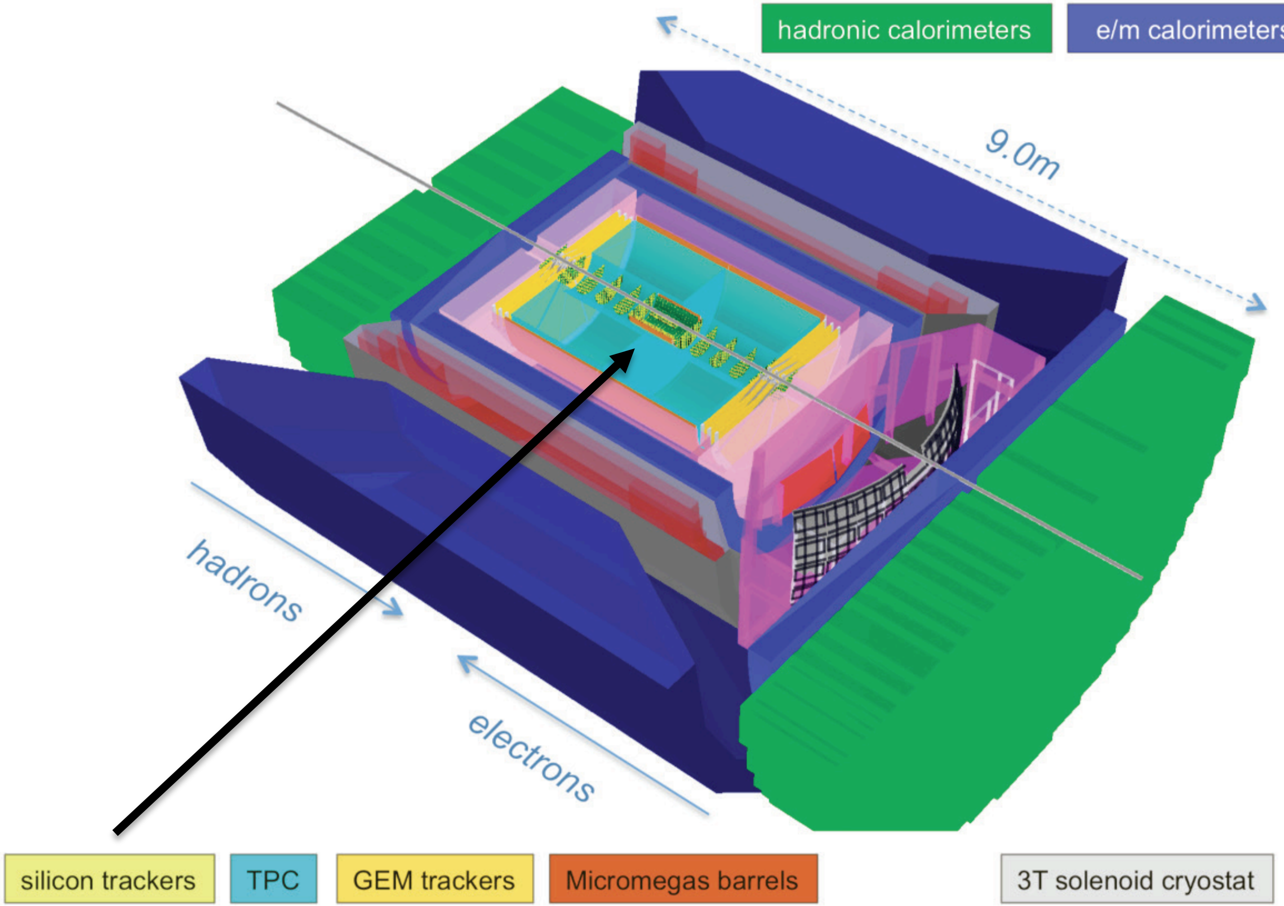
EIC detector requirements

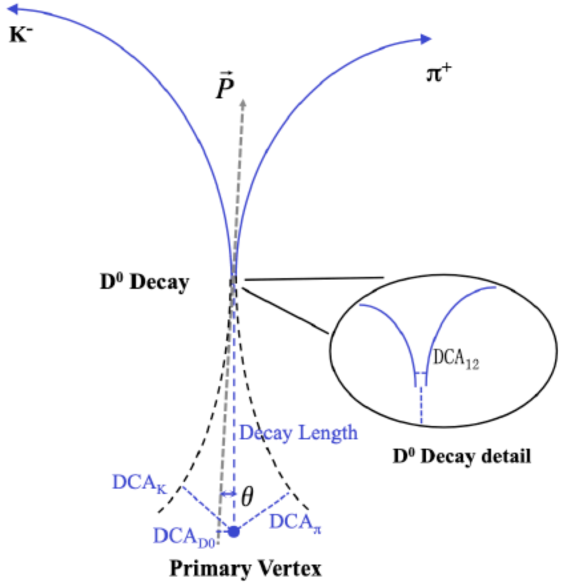
EIC Detector Requirements

η	Nomenclature			Tracking: Resolution	Tracking: Allowed X/X_0	Tracking: Si-Vertex	Electrons: Resolution σ_E/E	Electrons: PID	π/K/p PID: p-Range (GeV/c)	π/K/p PID: Separation	HCAL: Resolution σ_E/E	Muons
-6.9 — -5.8	↓ p/A	Auxiliary Detectors	low-Q^2 tagger	$\delta\theta/\theta < 1.5\%$; $10^{-6} < Q^2 < 10^{-2}$ GeV^2								
…												
-4.5 — -4.0			Instrumentation to separate charged particles from photons				2%/√E					
-4.0 — -3.5												
-3.5 — -3.0		Central Detector	Backwards Detectors	$\sigma_p/p \sim 0.1\% \times p + 2.0\%$	~5% or less	TBD		π suppression up to	≤ 7 GeV/c		~50%/√E	
-3.0 — -2.5												
-2.5 — -2.0				$\sigma_p/p \sim 0.05\% \times p + 1.0\%$								
-2.0 — -1.5							7%/√E					
-1.5 — -1.0												
-1.0 — -0.5			Barrel	$\sigma_p/p \sim 0.05\% \times p + 0.5\%$		$\sigma_{xyz} \sim 20$ μm, $d_0(z) \sim d_0(r\phi) \sim 20/p_T$ GeV μm + 5 μm	(10-12)%/√E					
-0.5 — 0.0												
0.0 — 0.5												
0.5 — 1.0												
1.0 — 1.5			Forward Detectors	$\sigma_p/p \sim 0.05\% \times p + 1.0\%$		TBD						
1.5 — 2.0												
2.0 — 2.5												
2.5 — 3.0				$\sigma_p/p \sim 0.1\% \times p + 2.0\%$								
3.0 — 3.5												
3.5 — 4.0	↑e	Auxiliary Detectors	Instrumentation to separate charged particles from photons									
4.0 — 4.5												
…												
> 6.2			Proton Spectrometer	$\sigma_{intrinsic}(\|t\|)/\|t\| < 1\%$; Acceptance: $0.2 < p_T < 1.2$ GeV/c								

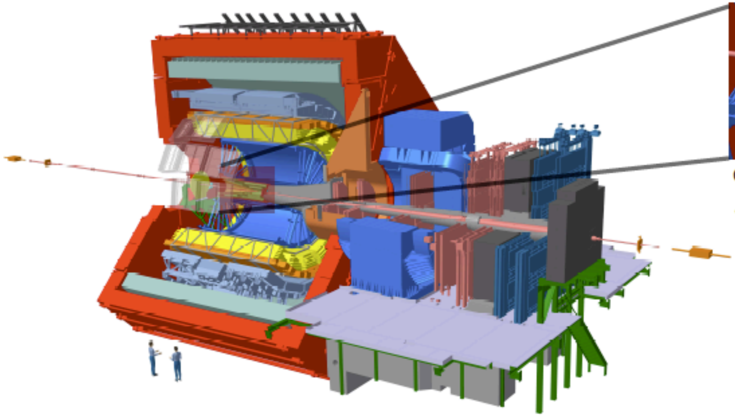


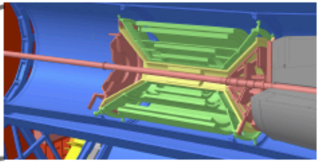
Silicon detector for heavy-flavor measurements





ALPIDE for ALICE ITS2 and sPHENIX MVTX

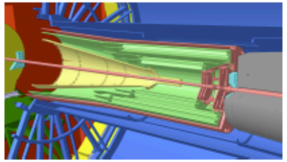




Current ITS

- 6 Layers
  - 2 Silicon Pixel
  - 2 Silicon Drift
  - 2 Silicon Strip

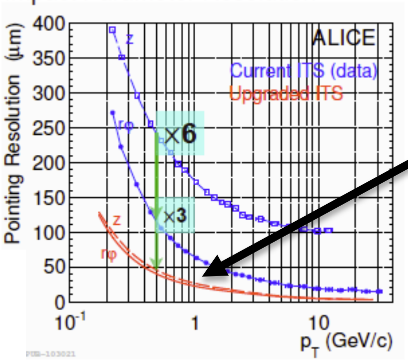
LHC LS2
2019-2020



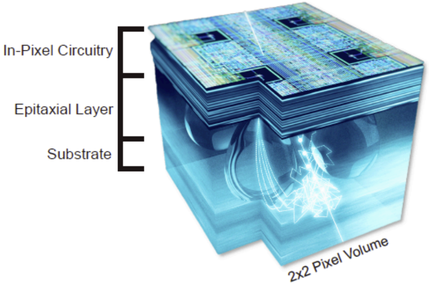
Upgraded ITS (**ITS2**)

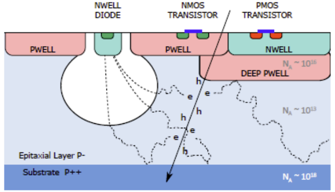
- 7 Layers
  - All Silicon Pixels
  - MAPS Technology
  - Chip thickness
    - Inner 3 layers : 50μm
    - Outer 4 layers : 100μm

Improvement of
Impact Parameter Resolution



- MAPS (Monolithic Active Pixel Sensor) Technology
- Material Budget X : $\mathbf{1.14\%X_0 \rightarrow 0.3\%X_0}$





Simple Schematic for Silicon Pixel Detector

ALPIDE sensor
180 nm Tower Jazz
28 x 28 μm² pixel pitch
~ 5 μs integration time
Power density **40 mW cm⁻²**
50 kHz interaction rate (Pb-Pb)
200 kHz interaction rate (pp)

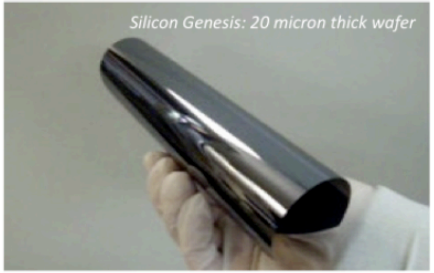
η	Si-Vertex
-6.9 — -5.8	
...	
-4.5 — -4.0	
-4.0 — -3.5	
-3.5 — -3.0	
-3.0 — -2.5	
-2.5 — -2.0	TBD
-2.0 — -1.5	
-1.5 — -1.0	
-1.0 — -0.5	
-0.5 — 0.0	σ_{xyz} ~ 20 μm, $d_0(z) \sim d_0(r\phi)$ ~ $20/p_T$ GeV μm + 5 μm
0.0 — 0.5	
0.5 — 1.0	
1.0 — 1.5	
1.5 — 2.0	
2.0 — 2.5	TBD
2.5 — 3.0	
3.0 — 3.5	
3.5 — 4.0	
4.0 — 4.5	
...	
> 6.2	

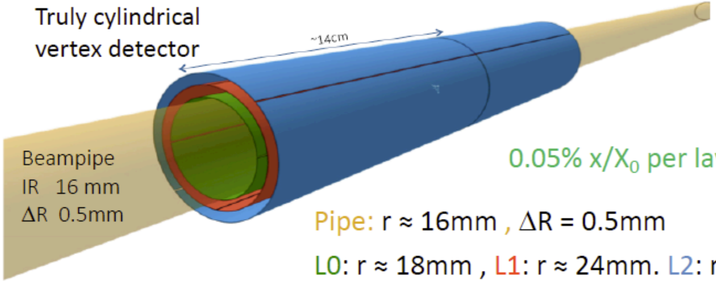
Interaction frequency = 50 - 500 kHz ➔ integration time down to 2 μs

ALICE ITS3

Recent silicon technologies (ultra-thin wafer-scale sensors) allow

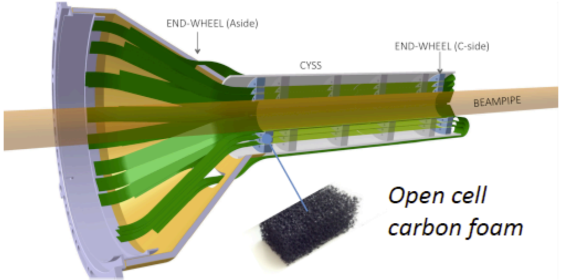
- Eliminate active cooling ⇨ possible for power < $20mW/cm^2$
- Eliminate electrical substrate ⇨ Possible if sensor covers the full stave length
- Sensors arranged with a perfectly cylindrical shape ⇨ sensors thinned to ~30µm can be curved to a radius of 10-20mm

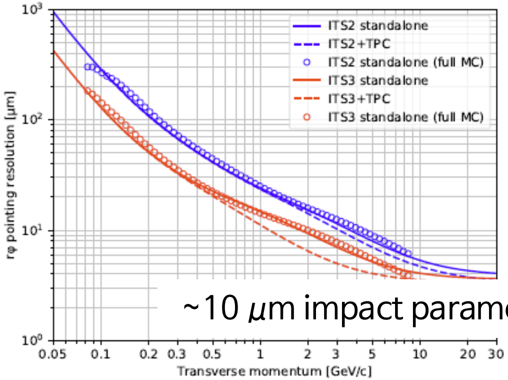


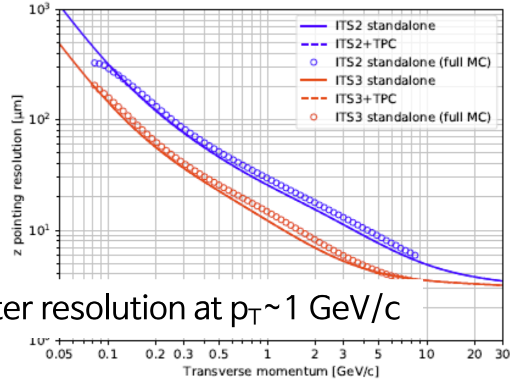


Pipe: $r \approx 16mm$, $\Delta R = 0.5mm$

L0: $r \approx 18mm$, L1: $r \approx 24mm$. L2: $r \approx 30$ mm







~10 µm impact parameter resolution at p_T~1 GeV/c

Specifications

Parameter	ALPIDE (existing)	Wafer-scale sensor (this proposal)
Technology node	180 nm	65 nm
Silicon thickness	50 µm	20-40 µm
Pixel size	27 x 29 µm	O(10 x 10 µm)
Chip dimensions	1.5 x 3.0 cm	scalable up to 28 x 10 cm
Front-end pulse duration	~ 5 µs	~ 200 ns
Time resolution	~ 1 µs	< 100 ns (option: <10ns)
Max particle fluence	100 MHz/cm^2	100 MHz/cm^2
Max particle readout rate	10 MHz/cm^2	100 MHz/cm^2
Power Consumption	40 mW/cm^2	< 20 mW/cm^2 (pixel matrix)
Detection efficiency	> 99%	> 99%
Fake hit rate	< 10^{-7} event/pixel	< 10^{-7} event/pixel
NIEL radiation tolerance	~3 x 10^{13} 1 MeV n_{eq}/cm^2	10^{14} 1 MeV n_{eq}/cm^2
TID radiation tolerance	3 MRad	10 MRad

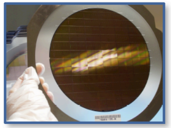
Production of ALPIDE

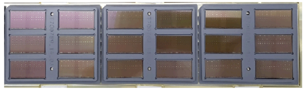
1500 raw wafers — **Raw Wafer Production** → 1% → **Raw Wafer QA** TMEC (Thailand)

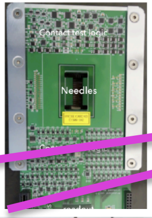
1200 CMOS wafers — **CMOS Manufacturing** TowerJazz (Israel) → 8% (2/25) → **Wafer Probe Testing** CERN

60 000 chips — **Thinning & Dicing** FUREX (South Korea)

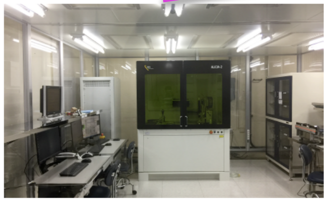
Pick & Place FUREX (South Korea) → 100% → **Chip Series Testing** Yonsei, Pusan/Inha (South Korea)

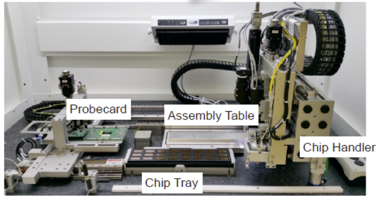


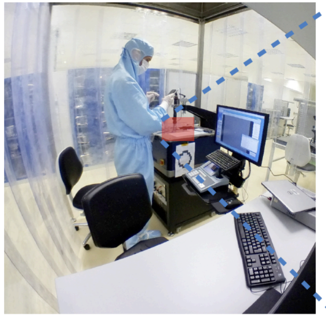




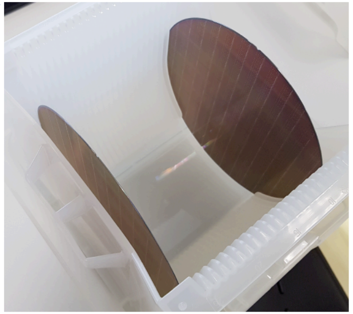
Module Assembly



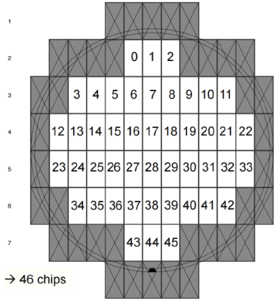




CERN
Wafer Probe Testing

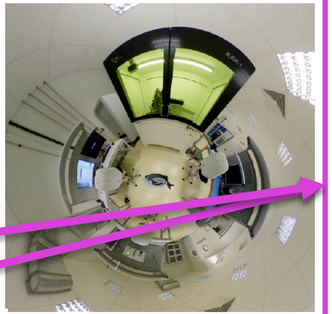


Imaged Wafer



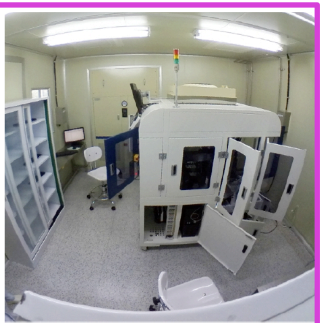
Dicing Diagram

Chip Test Sites



CERN
Chip Test and IB HIC Assembly
50μm ALPIDE

Pusan/Inha
Chip Test and OB HIC Assembly
100μm ALPIDE



Yonsei
Chip Test
100μm ALPIDE

BACKUP